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1461

B. E. - II Year (Sem. III) Examination, December – 2007

Digital Electronics

(Common to Computer Engg. & IT)

Time : 3 Hours] [Total Marks : 80

[Min. Passing Marks : 24

*Attempt overall **5** questions selecting **one** question from each unit.*
*All questions carry **equal** marks.*

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. Nil 2. Nil

1 (a) (i) Assume that X is 2's complement of n-bit binary number Y. Prove that 2's complement of X is Y. 4

(ii) Find equivalent binary Gray code of $(478)_{10}$. 4

(b) Minimize the following Boolean expressions using basic laws of Boolean algebra :

(i) $Y = AB + \overline{AC} + A\overline{B}C\left(AB + C\right)$

(ii) $Y = \overline{\left(AB + \overline{C}\right) + \left(\overline{A + B + C}\right)}$ 8

OR

1 (a) Subtract the following using 9's complement method :

(i) $649 - 387$

(ii) $891 - 786$

4

(b) (i) $(110101)_G = (?)_2$

(ii) $(10101101)_2 = (?)_G$

4

(c) What range of number can be represented in

(i) 8-bit sign magnitude form ?

(ii) 8-bit unsigned magnitude form ?

(iii) 8-bit BCD ?

(iv) 8-bit 2's complement form ?

8

2 (a) Express the function $Y = A + \overline{B}\,C$ in :

(i) Canonical SOP form

(ii) Canonical POS form.

6

(b) Using K-map method, simplify the following Boolean function and obtain :

(i) minimal SOP form

(ii) minimal POS form

$$Y = \Sigma_m(0, 2, 3, 6, 7) + \Sigma_d(8, 10, 11, 15)$$

10

OR

2 (a) Obtain the minimal SOP expression for the function

$$Y = \Sigma_m (1, 5, 7, 13, 14, 15, 17, 18, 21, 22, 25, 29) + \Sigma_d (6, 9, 19, 23, 30)$$

8

(b) Find minimal SOP form for the function $f = \Sigma(1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$ using the Quine McCluskey method.

8

3 (a) Design a full adder using 4×1 multiplexer.

6

(b) Design a four input priority encoder.

6

(c) Write VHDL code for

(i) NAND gate

(ii) Half adder.

4

OR

3 (a) Design a BCD adder.

8

(b) Write VHDL code for a BCD to 7-segment decoder.

8

4 (a) Explain the construction and working of master-slave JK flip flop.

8

(b) Design a JK flip flop using T flip flop.

8

OR

4	(a)	What are various types of triggering of flip flops ? Explain them in detail.	6
	(b)	Design a sequence detector that detects '1101' at its input. Overlapping sequences are acceptable. (Use D-flip flops)	10

5	(a)	Define the following characteristics of digial ICs. (i) Propagation delay (ii) Power dissipation (iii) Fan in (iv) Noise Margin.	12
	(b)	What are major advantages of totem-pole output arrangement ?	4

OR

5	(a)	Explain the operation of tri-state TTL NAND gate with the help of a neat diagram.	8
	(b)	Compare the characteristics of RTL, TTL, ECL and CMOS logic families.	8