5E5041

Roll No. _____ Total No of Pages: 3

5E5041

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical & Electronics Engineering
5EX1A Power Electronics
EX, EE

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) What are the differences in the gating characteristics of thyristors & transistors? [8]

(b) What are the differences between enhancement type MOSFETs & depletion type MOSFETs? [8]

OR

Q.1 (a) Briefly explain the V – I characteristics of an IGBT. [8]

(b) Give the merits & demerits of a GTO as compared to a conventional SCR. [8]

UNIT – II

Q.2 (a) The gate circuit of an SCR has a source voltage of 15V & the load line has a slop of –120V per ampere. The minimum gate current to turn-on the SCR is 25mA. Calculate: [8]

(i) Gate – source resistance R_S.

(ii) The gate voltage & gate current for an average gate power dissipation of 0.4 watts.

(b) What is the purpose of having parallel operation of SCRs? What care must be taken when paralleling the SCRs? [8]

OR

Q.2 (a) Explain the various types of triggering methods of SCR briefly. Which is the universal method & why? [8]

(b) What are $\frac{dv}{dt}$ & $\frac{di}{dt}$ rating of SCRs? What happens if these rating are exceeded? Explain. [8]

UNIT – III

Q.3 (a) Explain with a neat circuit diagram the basic principle of a dual converter. [8]

(b) For 3 – ϕ full converter operating from 3- ϕ, 415/50H_Z supply, determine & plot the following - [8]

(i) Fundamental component of the supply current.

(ii) 5^{th}, 7^{th}, 11^{th}, & 13^{th} harmonics for $\propto = 0°, 30°, 60°, 90°, 120°, 150°$.

Assume large inductive load with $R_L = 10\ \Omega$.

OR

Q.3 (a) Describe working of a single phase full converter with RLE load through the waveform of supply voltage, load voltage, load current & voltage across thyristor. Also derive expression for load voltage & input power factor. [8]

(b) A single- phase half- wave controlled converter is operated from a 120V, 50Hz supply. Load resistance R = 10 Ω. If the average output voltage is 25% of the minimum possible average output voltage, determine: – [8]

(i) Firing angle

(ii) rms & average output current

(iii) rms & average SCR current

UNIT – IV

Q.4 (a) Explain with associated waveform, how power factor can be improved with symmetrical angle control scheme. [8]

(b) A single-phase semi converter is operated from 200V, 50Hz source. If load resistance R = 8Ω & source has an inductance of 1.5mH, for an firing angle delay of 60°, determine: – [8]

(i) Average output voltage

(ii) The angle of overlap.

OR

Q.4 (a) Explain in detail the sinusoidal pulse width modulation control scheme for power factor improvement. [8]

(b) Describe the working of a single phase semi converter with RL load, through the waveform of supply voltage, load voltage, load current & voltage across thyristor & also derive expression for load voltage & input power factor. [8]

UNIT – V

Q.5 (a) What is the principle of operation of a step down chopper? [8]

(b) A DC chopper circuit connected to a 100V DC source supplies an inductive load having 40mH in series with a resistance of 5Ω. A free wheeling diode is placed across the load. The load current varies between the limits of 10A & 12A. Determine the time ratio of the chopper. [8]

OR

Q.5 (a) Explain multiphase chopper along with relevant circuit diagram & waveform. [8]

(b) Explain working principle of type–A chopper along with relevant circuit diagram & waveform. [8]

5E5042

Roll No. _____ Total No of Pages: 3

5E5042

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical Engineering
5EE2A Microprocessors & Computer Architecture

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question from each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain In detail, 8085 Microprocessor architecture with its working phenomena and usefulness. [8]

(b) Explain the following with respect to microprocessor architecture: [8]

(i) CPU

(ii) Address bus

(iii) Data Bus

(iv) Control bus

OR

Q.1 (a) Describe by help of a suitable diagram the pin definitions of 8085. [8]

(b) What are peripheral devices? Also explain the concept of memory organization for microprocessor. [8]

UNIT – II

Q.2 (a) Explain various instruction clarification for 8085 microprocessor. [8]

(b) Explain Instruction & opcode formats for 8085. [8]

OR

Q.2 (a) Draw the flow chart and write instruction to multiply two 8-bit numbers. [8]

(b) Write short note on counter & time delay. [8]

UNIT – III

Q.3 (a) With the help of a suitable block diagram explain the interfacing of 8255 chips, and its application. [8]

(b) Explain the utilization and interference techniques of 8259. [8]

OR

Q.3 (a) Explain the concept of keyboard interfacing for 8279. [8]

(b) By help of suitable diagram explain the concept of A/D conversion' in 8279. [8]

UNIT – IV

Q.4 (a) Explain the architecture of Intel 8086 and explain its bus interface unit & execution unit. [8]

(b) For 8086, microprocessor architecture explain the memory addressing & memory segmentation. [8]

OR

Q.4 (a) With reference to instruction set of 8086 explain addressing mode & processor control. [8]

(b) Explain hardware & software interrupts & response of 8086. [8]

UNIT – V

Q.5 (a) Explain the Basic Central Processing Unit with help of diagram. Also explain its need & application. [8]

(b) Explain the following type of memory - [8]

(i) Static & Dynamic memory.

(ii) Primary & Secondary memory.

OR

Q.5 (a) Explain ROM architecture and different type of ROM in detail. [8]

(b) Write short note on: [8]

(i) SDRAM, RDRAM

(ii) Flash & cache memory

5E5043

Roll No. _____ Total No of Pages: 4

5E5043

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical Engineering
5EE3A Control Systems

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

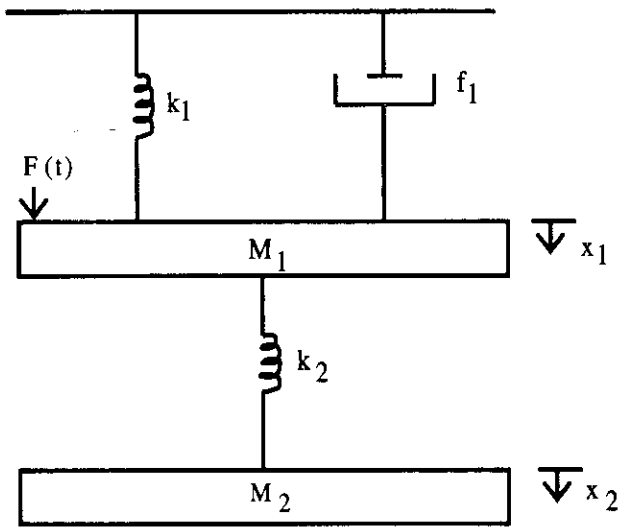
Q.1 (a) Determine the pole zero location of the following transfer function. [6]

(i) $s_1(t) = e^{-at}$; a decaying exponential

(ii) $s_2(t) = \cos wt$

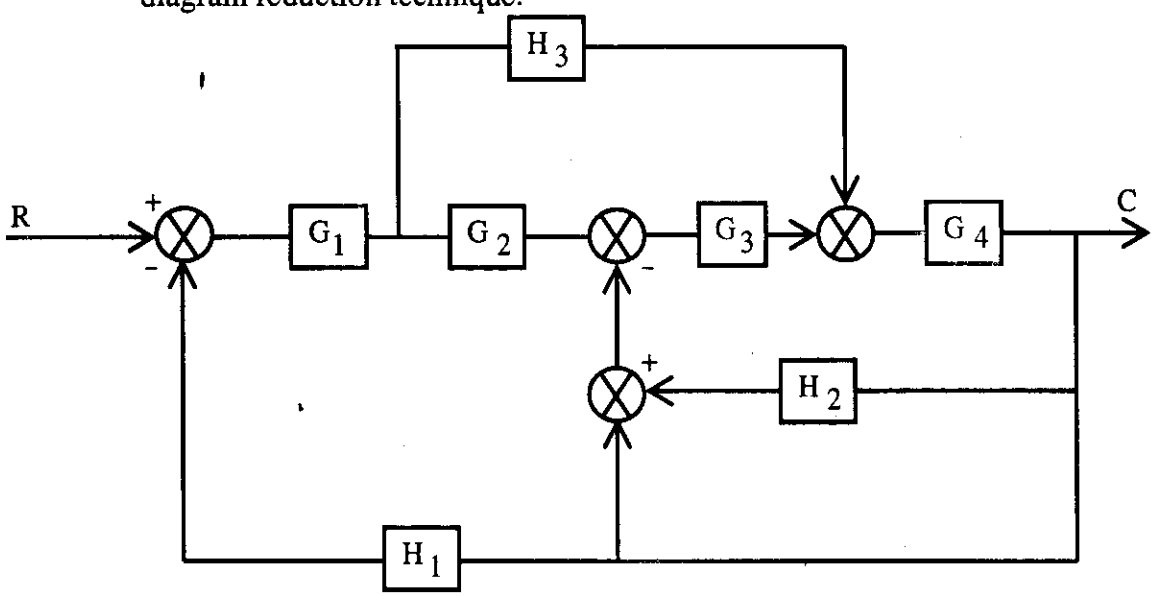
(iii) $s_3(t) = e^{-at} \cos wt$

(b) Determine system equation of the system shown in figure below. Also draw force – current analogy. [10]

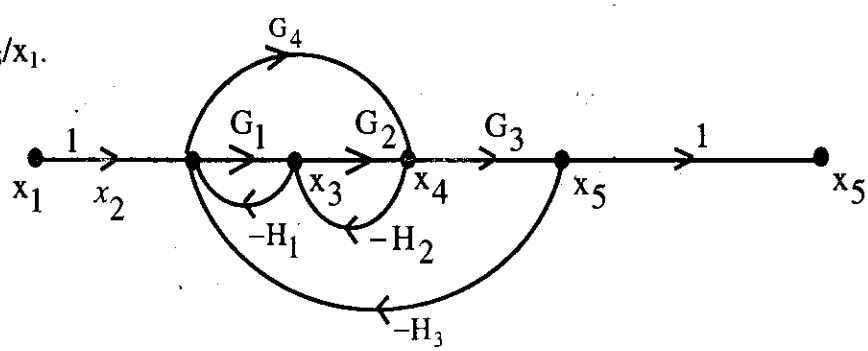


OR

Q.1 (a) Obtain the transfer function of the block diagram shown below using block – diagram reduction technique. [10]



(b) Apply the gain formula to the signal flow graph show in figure to find transfer function x_5/x_1. [6]



UNIT – II

Q.2 (a) Explain the effect of adding pole and zeros to transfer function. [6]

(b) A second order control system is represented by a transfer function given below. [10]

$$\frac{Q_o(s)}{T(s)} = \frac{1}{Js^2 + Fs + K}$$

Where $Q_o(s)$ is proportional output and T is the input torque.

A step input 10 N-m is applied to the system and test results are given below:-

(i) Peak overshoot Mp = 6%

(ii) Peak time tp = 1sec.

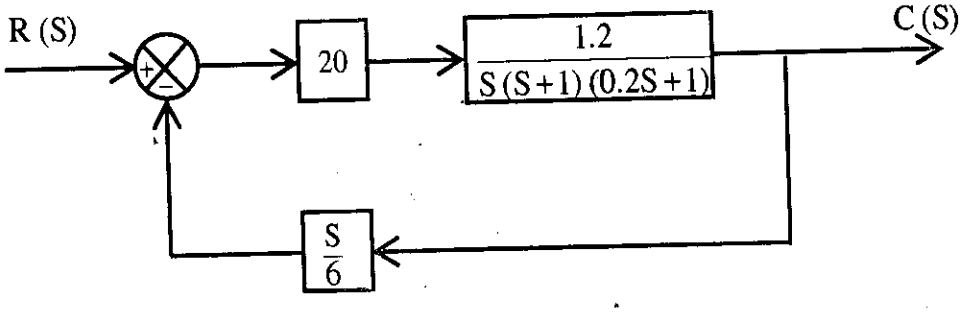
(iii) The steady state output of the system is 0.5 radian.

OR

Q.2 (a) Determine the step, ramp and parabolic error constant of the following unity feedback control system. The open loop transfer function is given by - [6]

$$G(s) = \frac{50}{S(s^2 + 5s + 50)}$$

(b) The block diagram of simple servo system is shown below. Find - [10]



(i) The characteristics equation of the system.

(ii) Undamped frequency of oscillation.

(iii) Damped frequency of oscillation.

(iv) Damping ratio.

(v) Maximum overshoot.

UNIT – III

Q.3 (a) Explain the construction and working of stepper motor. [8]

(b) Using the Routh Criterion check whether the system represented by the following characteristic equation is stable or not. [8]

$S^4 + 2s^3 + 6s^2 + 8s + 8 = 0$

OR

Q.3 (a) Sketch the root locus with K as a variable parameter of a unity feedback system whose open loop transfer function is - [10]

$$G(s) = \frac{k(s+2)}{s^2+2s+3}$$

(b) Determine the range of valve of K for the system to be stable - [6]

$s^4 + 4s^3 + 13s^2 + 36s + K = 0$

UNIT – IV

Q.4 (a) Draw the Nyquist plot for a system having [10]

$$G(s)\,H(s) = \frac{s+4}{(s+1)(s-1)}$$

Use Nyquist criterion to determine the system stability.

Q.4 (b) Explain co–relation between time and frequency response. [6]

OR

Q.4 Draw the bode plot for the transfer function - [16]

$$G(s) = \frac{50}{s(1+0.25s)(1+0.1s)}$$

From the plot determine gain margin and phase margin.

UNIT – V

Q.5 (a) Derive the formula for steady state error (e_{ss}) of P. I. Control [8]

(b) Write down the merits and demerits of Phase-Lag-Lead Compensation. [8]

OR

Q.5 Compensate the system with the Open Loop Transfer Function - [16]

$$G_f(s) = \frac{k}{s(s+1)(s+5)}$$

to meet following specification:-

(a) Damping ratio (ε) = 0.3

(b) Settling time (t_s) = 12 sec.

(c) Velocity error constant $k_v \geq 8\ sec^{-1}$

5E5044

Roll No. _____ Total No of Pages: 4

5E5044

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical & Electronics Engineering
5EX4A Database Management System
EE, EX

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. NIL

UNIT – I

Q.1 (a) What is DBMS? Explain purpose and goals of DBMS and also draw the overall architecture of DBMS and explain its various components. [7]

(b) Define the following terms – [3×3=9]

(i) Primary key & Foreign key

(ii) ER Modeling

(iii) Generalization and Aggregation

OR

Q.1 (a) Design on E-R diagram for "Tourism" system consisting of Transport, Place, attractions, accommodation, info tourist. Clearly highlight the primary keys and mapping cardinalities. [7]

(b) Differentiate between the following –

(i) Candidate key and super key.

(ii) Entity sets, Attributes and Relationship sets.

(iii) Ternary Relationship and Aggregation. [3×3=9]

UNIT – II

Q.2 (a) What is Normalization? Explain its need. Define various normal forms with example. [8]

(b) Explain the following terms –

(i) Physical & Logical databases

(ii) Relational Algebra and Relational calculus. [4×2=8]

OR

Q.2 (a) How does Boyce – Codd normal form differ from 3NF? Why is it considered stronger from 3NF? Also discuss 4NF and 5NF with suitable example. [7]

(b) Define the following – [3×3=9]

(i) Multivalued Dependency

(ii) Functional Dependency

(iii) Lossless Decomposition

UNIT – III

Q.3 (a) What do you mean by query and sub query? Discuss the various characteristics of SQL and explain five aggregate functions with suitable example. [8]

(b) Explain the following – [2×4=8]

(i) ORDER BY

(ii) GROUP BY

(iii) LIKE

(iv) EXCEPT

OR

Q.3 (a) What is a view? How a view be used to implement database security? Explain with example. [8]

(b) Explain in detail: [4×2=8]

(i) Stored procedures and Triggers

(ii) JDBC and Dynamic SQL

UNIT – IV

Q.4 (a) What are the various types of indexes? Explain with examples. [6]

(b) What do you mean by schedule in the context of concurrent execution of transactions in RDBMS? Discuss physical data organization in sequential indexed, random and hashed files. [10]

150

OR

Q.4 (a) **What is physical data organization in sequential and how does it work.** [8]

(b) **Explain inverted and multi list structures.** [8]

UNIT – V

Q.5 (a) Define transaction management? What are the properties of transaction? Explain in detail. [8]

(b) Define Serializability. What are its various types? [8]

OR

Q.5 (a) What is a Deadlock? Explain various techniques of handling deadlocks. [8]

(b) What is concurrency control: Lock based protocol? Explain with example. [8]

151

5E5045

Roll No. _____ Total No of Pages: 3

5E5045

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical & Electronics Engineering
5EX5A Transmission & Distribution of Electrical Power

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) What is meant by the terms feeder, distribution and service mains? Why the distribution by A.C. is Considered to be superior to that by D.C.? [8]

(b) Prove that the volume of conductor required in a transmission system is inversely proportional to the square of the voltage as well as power factor of the load. State the condition under which this statement is true. [8]

OR

Q.1 (a) Compare DC 2 – wire and DC – 3 wire. [6]

(b) Explain the radial and ring main distribution system. [10]

UNIT – II

Q.2 (a) Derive an expression for sag of a line supported between two supports of same height. [8]

(b) What is meant by disruptive critical voltage and visual critical voltage? State the effects of conductor size, spacing and condition of the surface of conductor on these voltages. [8]

OR

Q.2 (a) Explain the necessity and method of preparing "Stringing charts" for over head transmission lines. [8]

(b) A transmission line has a span of 150m between level supports. The x – sectional area of the conductor is 1.25cm^2 and weight 100kg per 100m. If the breaking stress is 4220kg/cm^2, calculate the factor of safety if the sag of the line is 3.5m. Assume a maximum wind pressure of 100kg per sq. meter. [8]

UNIT – III

Q.3 (a) Prove that the inductance of a group of parallel wires carrying current can be represented in term of their geometric distance. Explain the meaning of the term "Self g.m.d. and Mutual g.m.d." [8]

(b) Explain skin and proximity effects. [8]

OR

Q.3 (a) Derive the capacitance of a three phase overhead line. [8]

(b) Derive an expression for capacitance of three phase transmission line with unsymmetrical spacing. [8]

UNIT – IV

Q.4 Explain the following:

(a) Corona power loss

(b) Electric stress between parallel conductors

OR

Q.4 (a) Derive an expression for the voltage induced in communication lines due to the current in power lines. [8]

(b) Find the value of A, B ,C and D in the following approximate methods interms of z and y. [8]

(i) Nominal π method

(ii) Nominal T – method

UNIT – V

Q.5 (a) A single core cable for use in 11kV, 50Hz system has conductor area of 0.645 cm^2 and the internal diameter of sheath is 2.18 cm. The permittivity of the dielectric used in the cable is 3.5. Find the maximum and minimum electrostatic stresses in the cable. [8]

(b) Explain any two methods of grading of cables with necessary diagram. [8]

OR

Q.5 Explain the following: [8+8=16]

(a) Oil filled and Gas filled cables

(b) Insulator resistance and capacitance calculation

5E5047

Roll No. _____ Total No of Pages: 3

5E5047

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical Engineering
5EE6.2A Principle of Communication System
EE, EX

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Derive noise figure in terms of available gain and derive the formula for noise figure of a cascade system. [8]

(b) A certain amplifier has input and output resistance of 50Ω and a noise equivalent bandwidth of 10KHz. When connected to a source and a matched load the net gain is 60dB. If a 50Ω resistor at 290°K is connected to the input, the output rms noise voltage across 50Ω is 80μV. Determine the equivalent noise temperature of the amplifier. [8]

OR

Q.1 (a) What is meant by noise figure and how can it be calculated for an amplifier or receiver? [8]

(b) Explain the concept of effective noise temperature of a network and equivalent noise bandwidth. [8]

UNIT – II

Q.2 (a) Draw the block diagram of phase discriminator method of generating SSB signal. [8]

(b) Describe mathematical analysis for coherent detection of baseband signal from SSB signal. [8]

OR

Q.2 (a) With the help of a circuit diagram explain the working of ring modulator for generating a DSB – SC signal. [8]

(b) For a modulation coefficient of M = 0.2 and a unmodulated carrier power P_C = 1000W, determine - [8]

(i) Total sideband power

(ii) Upper sideband power

(iii) Modulated carrier power

(iv) Total transmitted power

UNIT – III

Q.3 (a) Describe indirect method of FM generation. Compare it with the direct method.[8]

(b) Explain pre-emphasis and de-emphasis in FM broadcasting. [8]

OR

Q.3 (a) Explain FM demodulation using PLL using suitable mathematical expression. [8]

(b) An angle modulated signal is described by –

$x_c(t) = 10 \cos [2\pi (10^6) t] + 0.1 \sin (10^3) \pi t$ [8]

(i) Considerly $x_c(t)$ as a PM signal with KP = 10, find m(t)

(ii) Considerly $x_c(t)$ as a FM signal with Kf = 10π, find m(t)

UNIT – IV

Q.4 (a) Describe the function of super heterodyne radio receiver with block diagram. [8]

(b) Derive an expression for SNR of a FM demodulator. [8]

OR

Q.4 (a) Calculate S/N ratio in square law demodulator. [8]

(b) Calculate the signal to noise ratio for a double side band (DSB) with carrier signal. Obtain its figure of merit. [8]

UNIT – V

Q.5 (a) What is sampling theorem? Explain the statement of sampling theorem and mathematical proof. [8]

(b) Differentiate between Ideal, Natural and Flat Top sampling. [8]

OR

Q.5 (a) Discuss PAM – TDM using suitable block diagram. [8]

(b) Write short note on any two - [4x2=8]

(i) PAM

(ii) PWM

(iii) PPM

157

5E5048

Roll No. _____ Total No of Pages: 3

5E5048

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electrical & Electronics Engineering
5EX6.3A Introduction to VLSI
Common with EX EE

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Derive the V-I characteristics of enhancement MOSFET. [8]

(i) Ohmic region

(ii) Saturation region

(b) Explain the PMOS fabrication process in detail using suitable diagram. [8]

OR

Q.1 (a) Explain depletion mode MOSFET using suitable diagram [8]

(b) Explain the Twin – Tub CMOS fabrication process using suitable diagram. [8]

UNIT – II

Q.2 (a) Explain significance of $\left(\frac{\beta n}{\beta P}\right)$ ratio for a CMOS inverter. [8]

(b) What are the factors which effect the threshold voltage? Derive expression for threshold voltage. [8]

OR

Q.2 (a) Prove that the pull-up to pull down ratio for a NMOS inverter is 4:1, when it is driven by another inverter. [8]

(b) Derive $I_{ds} - V_{ds}$ relationship for MOSFET. [8]

UNIT – III

Q.3 Implement following gate using transmission gate. [4×4=16]

(a) OR gate

(b) AND gate

(c) NOR gate

(d) NAND gate

OR

Q.3 Realize the following logic expression using CMOS inverter. [4×4=16]

(a) $A.B + \overline{A}\,\overline{B}$

(b) $A.B\overline{C} + \overline{A}\,B\,C$

(c) $A.B\overline{C.D}$

(b) $AB + BC + AC$

UNIT – IV

Q.4 (a) Write a short note on "Layout optimization for performance". [8]

(b) Draw the stick diagram and layout for the following Boolean expression - [8]

$Y = A.B + C.D + E$

OR

Q.4 (a) Explain different types of layout design rules and compare them with application. [8]

(b) Draw the stick diagram of: [4+4=8]

(i) 3 I/P NAND gate

(ii) 3 I/P NOR gate

UNIT – V

Q.5 (a) Write VHDL code for 4:1 multiplexer in behavioral style of modeling. [8]

(b) Write VHDL code for full adder and full sub tractor. [8]

OR

Q.5 (a) Write VHDL code for 4 bits adder using full adder. [8]

(b) Explain package in VHDL. Explain difference between function and procedure. [8]

160

5E3126

Roll No. _____ Total No of Pages: 3

5E3126

B. Tech. V Sem. (Old Back) Exam., Nov.-Dec.-2016
Electrical Engineering
5EE4 (O) Generation of Electrical Power

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Distinguish between a breeder reactor and a converter reactor. Derive an expression for maximum conversion of fertile material in a converter reactor. [8]

(b) How can hydro plants be classified according to following? [8]

(i) Water flow regulation

(ii) Head & Load

OR

Q.1 (a) Briefly discuss the functions of following equipments in a steam station - [8]

(i) Condenser

(ii) Cooling towers

(iii) Economizer

(iv) Feed water heater

(b) Explain the basic schemes and working principle of Gas Power Plant with open cycle. [8]

UNIT – II

Q.2 (a) Explain the impact of thermal and hydro power station on environment. [8]

(b) How can solar energy be converted into electrical energy? Give a diagram showing the elements of such a plant. [8]

OR

Q.2 (a) Give a brief classification of various energy resources. What is the future of non – conventional energy sources in India? [8]

(b) What do you mean by Global Warming? What will happen due to it? [8]

UNIT – III

Q.3 (a) What are the disadvantages of low power factor? Explain the methods of power factor improvement. [8]

(b) Define the following terms for a power station: [8]

(i) Diversity factor

(ii) Load factor

(iii) Utilization factor

(iv) Annual plant capacity factor

OR

Q.3 (a) What is the difference between chronological curve and load duration curve? Explain the difference between base load and peak load also. [8]

(b) The maximum demand of power plant is 80 MW. The capacity factor is 0.5 and the utilization factor is 0.8. Find – [8]

(i) Load factor

(ii) Plant capacity

(iii) Reserve capacity

(iv) Annual energy production

UNIT – IV

Q.4 (a) Calculate the most economical power factor when KW demand is constant. [8]

(b) Explain the role of load diversity in power system economics. [8]

OR

Q.4 (a) Explain the concept of co- generation and energy conservation in terms of power plant economics. [8]

(b) Explain the capital cost, annual fixed and operating costs of plants. [8]

UNIT – V

Q.5 (a) Distinguish between operating reserve and spinning reserve. Explain why the size of power plant units have been continuously increasing for the past many years. [8]

(b) How do demand factor, load factor and diversity factor in a power system affect the fixation of tariffs? [8]

OR

Q.5 (a) Explain flat demand rate and straight meter rate in terms of Electrical tariff. [8]

(b) Describe in detail methods of selection and location of various power plants. [8]

5E3128

Roll No. _____ Total No of Pages: 2

5E3128

B. Tech. V Sem. (Old Back) Exam., Nov.-Dec.-2016
Electrical Engineering
5EE6.1 (O) Advanced Distribution Systems

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question from each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 Explain load forecasting – regression analysis in detail along with correlation theory. [16]

OR

Q.1 Write short notes on:

(a) Future distribution systems [8]

(b) Load growth factors [8]

UNIT – II

Q.2 Explain operation criterion and various standards in detail for voltage control. [16]

OR

Q.2 (a) Explain various effects of harmonics on networks. [8]

(b) What is Ferro resonance? Explain system losses in detail. [8]

UNIT – III

Q.3 (a) What is the role of monitoring and compensation in distribution system? Explain. [10]

(b) Give measures for maintaining system voltage. [6]

OR

Q.3 (a) Explain HT shunt capacitors in detail. [6]

(b) What is the difference between series and shunt capacitors? [5]

(c) Explain system harmonics in detail. [5]

UNIT – IV

Q.4 (a) What is the requirement of systems neutral earthing? Explain. [8]

(b) Explain earth fault protection of feeders in detail. [8]

OR

Q.4 (a) Explain the concept of earth electrode along with its design in detail. [9]

(b) Why earthing of substations is required? Explain. [7]

UNIT – V

Q.5 (a) Write and explain the concept of communication by power line carrier. [8]

(b) Explain distribution automation in detail. [8]

OR

Q.5 Explain following :–

(a) Satellite Communication & Sensors. [8]

(b) Supervisory Control and Data Acquisition. [8]
