3E1481

Roll No. : _____ Total Printed Pages : 7

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B.Tech. (Sem. III) (Main/Back) Examination, January - 2012
Electrical Engg.
3EE1 Power Electronics - I

Time : **3** Hours] [Total Marks : **80**
[Min. Passing Marks : **24**

Instructions to Candidates :

*Attempt any **five questions** selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

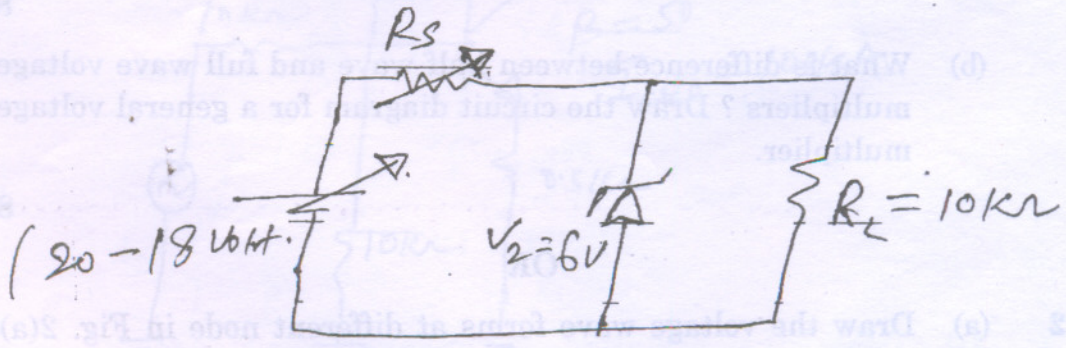
1. Nil 2. Nil

UNIT - I

1 (a) Explain the zener and avalanche breakdown mechanism in a breakdown diode. Draw the VI characteristic of such diode and modified the characteristics for different temperature.

4+4=8

(b) Design the range of source resistance Rs for regulate the voltage across the load in the circuit given in fig. 1(a)



I_{Zmin} = 20 kA
P_{Zmax} = 20 M watt 8

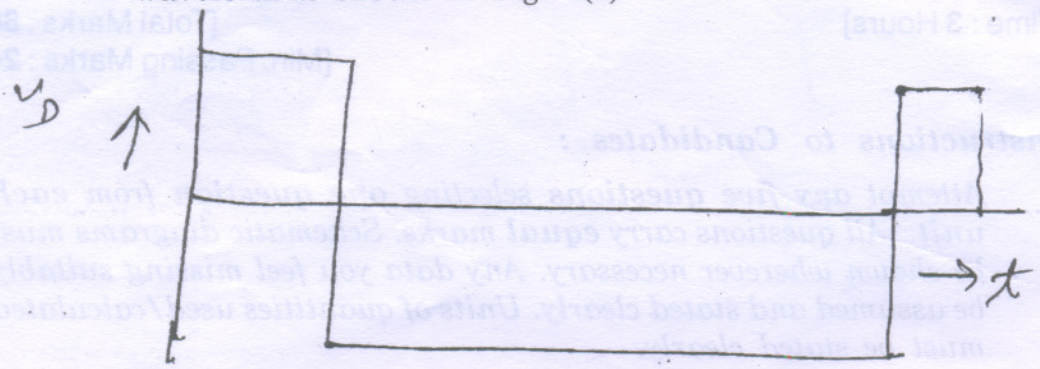
Fig. 1(a)

OR

1 (a) Find the expression for junction capacitance for a linear graded PN junction, draw it with applied reverse voltage.

8

(b) Draw the diode current for a applied voltage across diode, having finite $t_{on} = 10\ \mu\text{sec}$, $t_{off} = 50\ \mu\text{sec}$. The voltage waveform is shown in Fig. 1(b)



Explain the resons of delay and rise time for a semiconductor diode.

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UNIT - II

2 (a) Draw the AC and DC equivalent circuit of a PN junction and find the expression for corresponding diode resistance.

8

(b) What is difference between half wave and full wave voltage multipliers ? Draw the circuit diagram for a general voltage multiplier.

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OR

2 (a) Draw the voltage wave forms at different node in Fig. 2(a) modify the waveforms with different time consts (RC) as (i) RC = 0 (ii) RC = ∞ and (iii) RC = 2T.

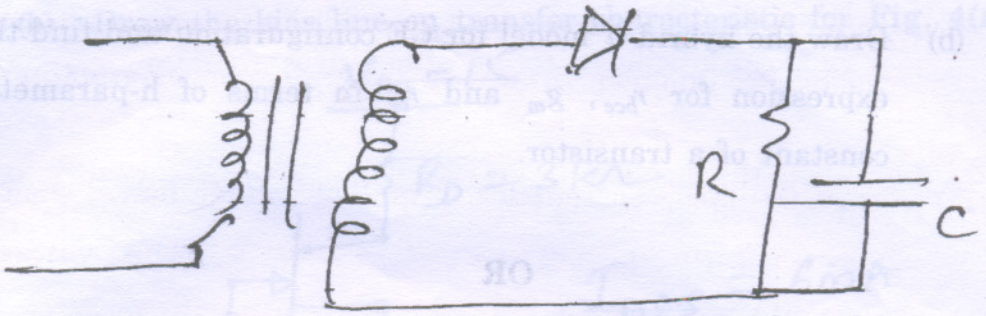

Fig. 2(a)

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(b) Draw the output voltage wave form for circuit Fig. 2 (b)

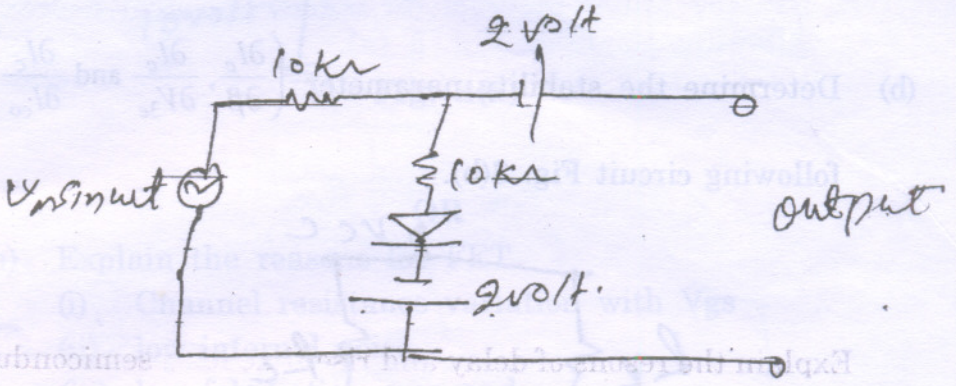

Fig. 2 (b)

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UNIT - III

3 (a) Find the operating point for the amplifier circuit Fig. 3(a)

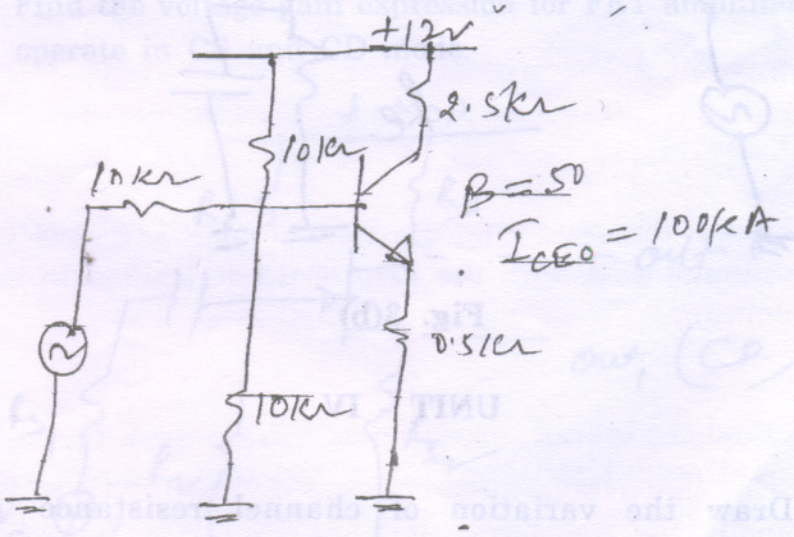

Fig. 3(a)

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(b) Draw the hybrid-$\hbar$ model for CE configuration and find the expression for r_{bce}, g_m and r_{ce} in terms of h-parameter constant of a transistor.

8

OR

3 (a) Draw the output and input characteristic for CB configuration and determine the h-parameter constants from these characteristic.

8

(b) Determine the stability parameter $\left(\frac{\partial I_c}{\partial \beta}, \frac{\partial I_c}{\partial V_{3e}} \text{ and } \frac{\partial I_c}{\partial I_{co}}\right)$ for following circuit Fig. 3(b).

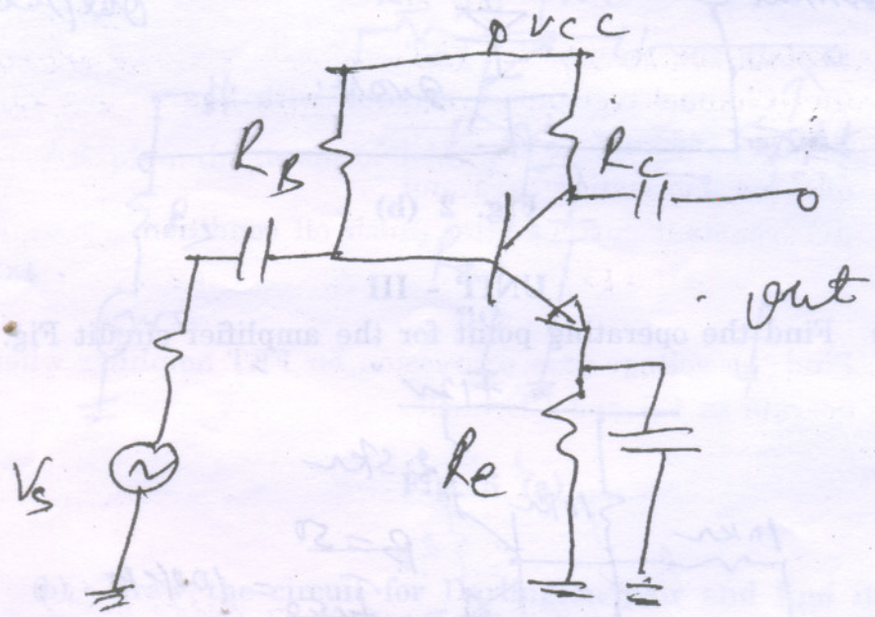

Fig. 3(b)

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UNIT - IV

4 (a) Draw the variation of channel resistance r_{ds} and trans-conductance g_m of a FET with (i) V_{gs} and (ii) V_{ds}.

4+4=8

(b) Draw the bias line on transfer characteristic for **Fig. 4(a)**

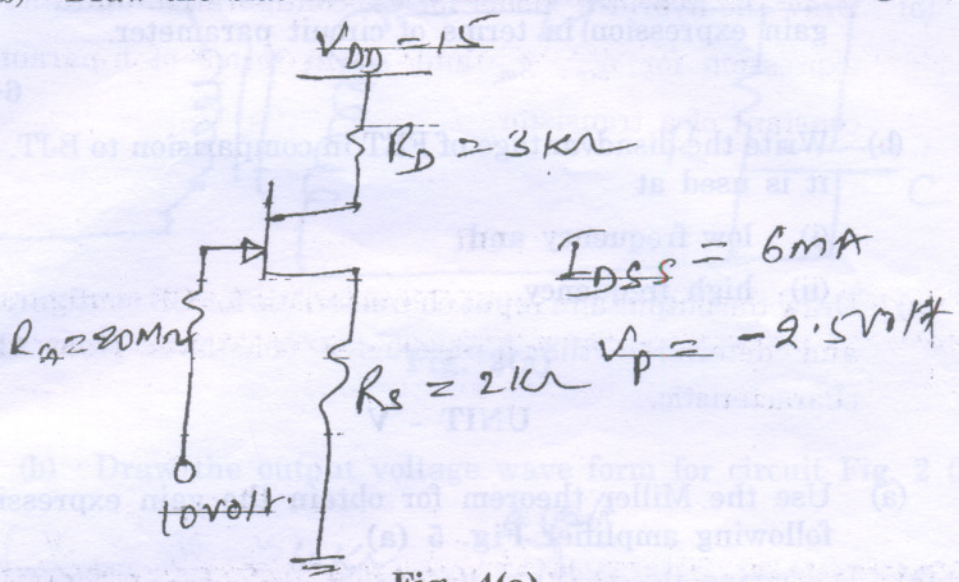

Fig. 4(a)

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OR

4 (a) Explain the reasons for FET

(i) Channel resistance variation with Vgs

(ii) low internal noise

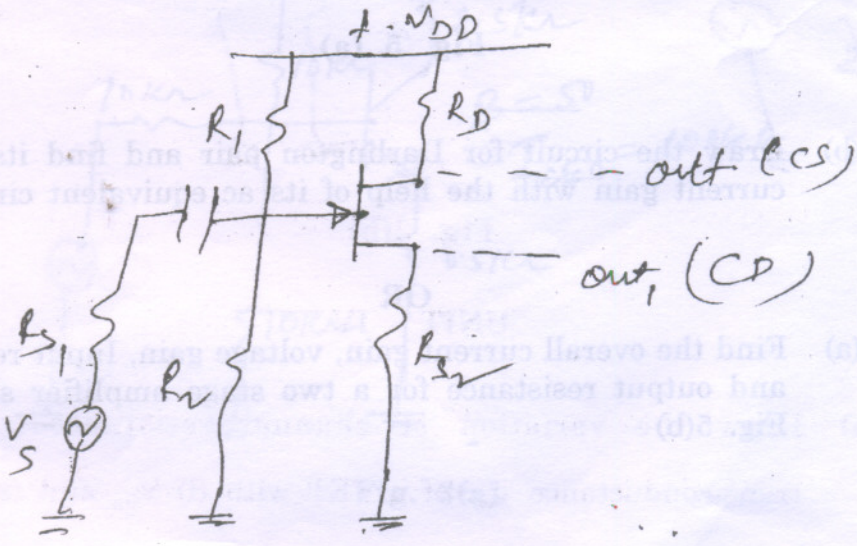
(iii) low fabrication area and

(iv) constant current after pinch off condition.

4×2=8

OR

4 (a) Find the voltage gain expression for FET amplifier when it operate in CS and CD mode.



Draw its AC equivalent circuit with FET model and find the gain expression in terms of circuit parameter.

6+6=12

(b) Write the disadvantage of FET in comparision to BJT. When it is used at

(i) low frequency and

(ii) high frequency.

2×2=4

UNIT - V

5 (a) Use the Miller theorem for obtain the gain expression in following amplifier **Fig. 5 (a)**.

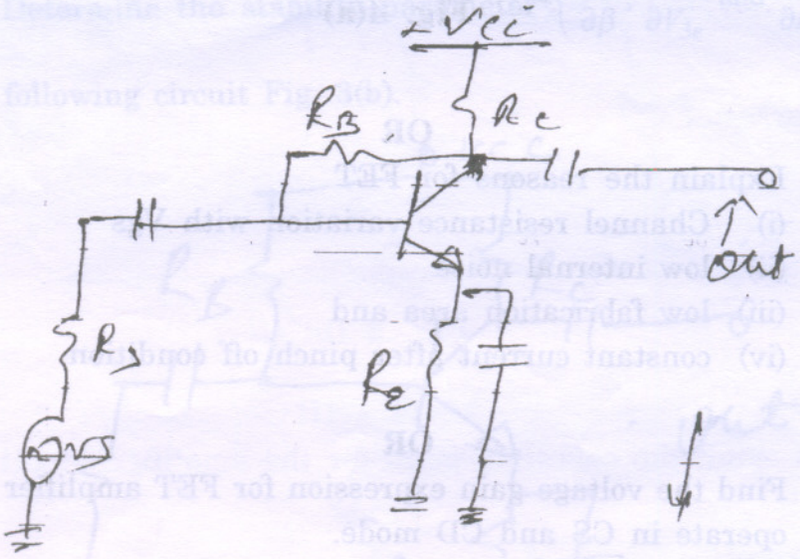


Fig. 5 (a)

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(b) Draw the circuit for Darlington pair and find its overall current gain with the help of its ac equivalent circuit.

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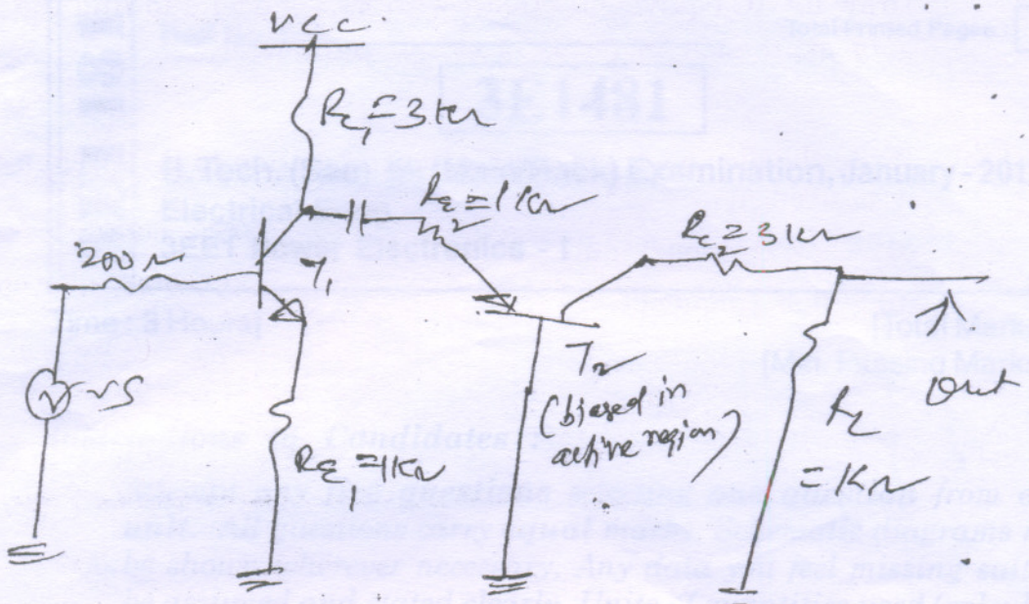
OR

5 (a) Find the overall current gain, voltage gain, Input resistance and output resistance for a two stage amplifier shown in Fig. 5(b)



Given

$h_{ie} = 1\,k\Omega \quad h_{fe} = 50$

$h_{oe} = 50\,V \quad h_{re} = 10$

Fig. 5(b)

5+5=10

(b) Compare the performance of CE-CE, CE-CB, CC-CE and CB-CC in tabluler form. **6**
