

3E1483

Roll No. : _____

Total Printed Pages : 7

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B.Tech. (Sem. III) (Main/Back) Examination, January - 2012

Electrical Engg.

3EE3 Circuit Analysis - I

Time : 3 Hours]

[Total Marks : 80

[Min. Passing Marks : 24

Instructions to Candidates :

Attempt any **five questions** selecting **one question** from each **unit**. All questions carry **equal marks**. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. _____ Nil _____ 2. _____ Nil _____

UNIT - I

1 (a) Draw the dual of the network as shown in Fig. 1.

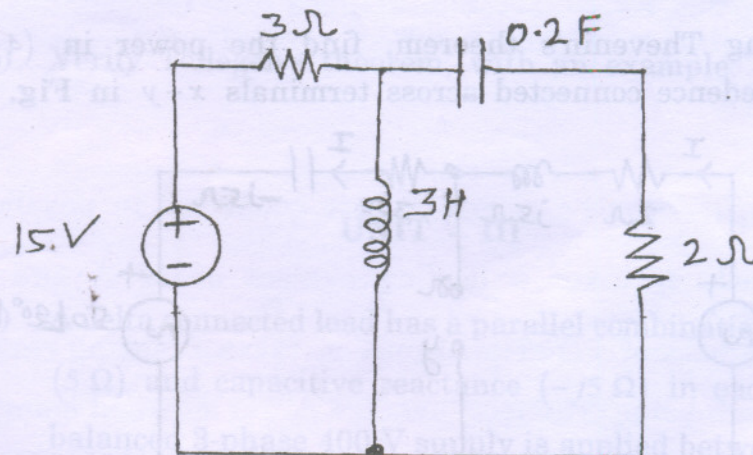


Fig. 1

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- (b) Obtain the fundamental loop and fundamental cut-set matrices for the graph shown in Fig. 2.

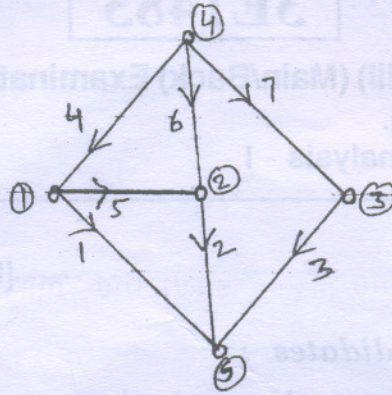


Fig. 2

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OR

- 1 (a) Define Q-factor in an AC circuit. Deduce the relation between bandwidth, resonant frequency and Q-factor.

2+6

- (b) A series RLC circuit has $R = 2 \Omega$, $L = 2.0 \text{ mH}$ and $C = 10 \mu\text{F}$. Calculate : (i) Q-factor of circuit (ii) the bandwidth (iii) Resonant frequency (iv) Half wave frequency f_1 and f_2 .

2×4=8

UNIT - II

- 2 (a) Using Thevenin's theorem, find the power in $(4 + j6) \Omega$ impedance connected across terminals x-y in Fig. 3.

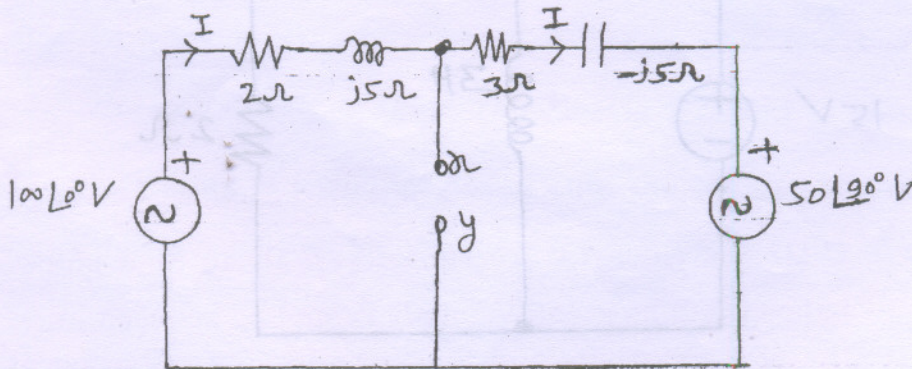
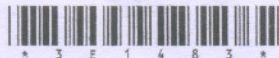


Fig. 3

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- (b) Prove that for a linear network containing generators and impedances, the ratio of a voltage V introduced in one loop to the current I produced in any other loop is same as the ratio of voltage and current obtained if the position of voltage source V and the current (I) measured are interchanged.

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OR

- 2 (a) Find the value of Z_L such that maximum power transfer takes place from source to Z_L in Fig. 4.

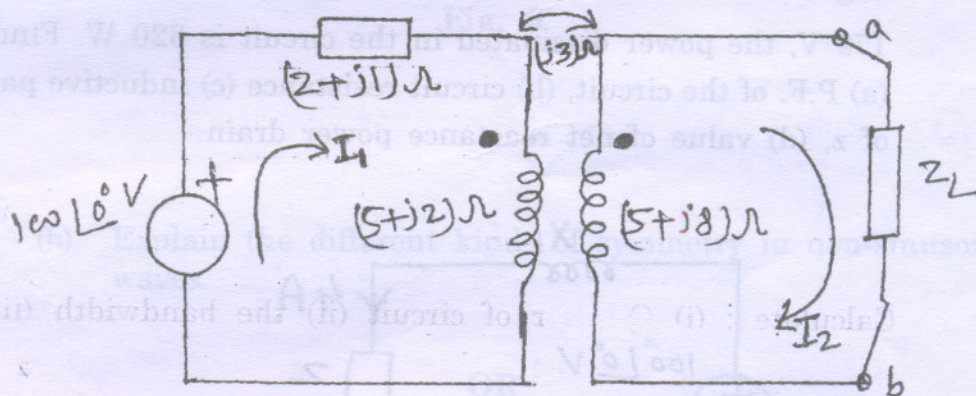


Fig. 4

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- (b) Verify Tellegen's theorem, with an example.

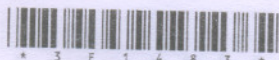
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UNIT - III

- 3 (a) A delta connected load has a parallel combination of resistance (5Ω) and capacitive reactance ($-j5 \Omega$) in each phase. If a balanced 3-phase 400 V supply is applied between lines, find the phase currents and line currents and draw the phasor diagram.

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- (b) Three identical resistances are connected in a star fashion against a balanced 3- ϕ voltage supply. If one of the resistance be removed, by how much the power be reduced ?

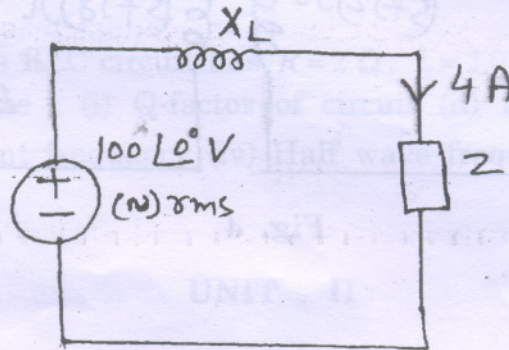
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- (c) Explain "neutral shifting" in unbalanced leading system of 3-phase.

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OR

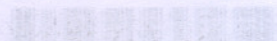
- 3 (a) The inductive reactance in series with Z in the circuit of Fig. 5 has a value of 25Ω . If the voltage drop across Z is 179 V, the power dissipated in the circuit is 320 W. Find : (a) P.F. of the circuit, (b) circuit resistance (c) inductive part of z , (d) value of net reactance power drain.



2×4=8

- (b) Two impedances z_1 and z_2 are connected in parallel. The branch z_1 takes a leading current of 16 A and has a resistance of 5Ω . The branch z_2 takes a lagging current of 0.8 p.f. value. The total average power supplied being 5 kW, applied voltage being $(100 + j200)V$, obtain the values of z_1 and z_2 and the total circuit current.

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UNIT - IV

- 4 (a) Obtain Fourier series of the given waveform in Fig. 6.

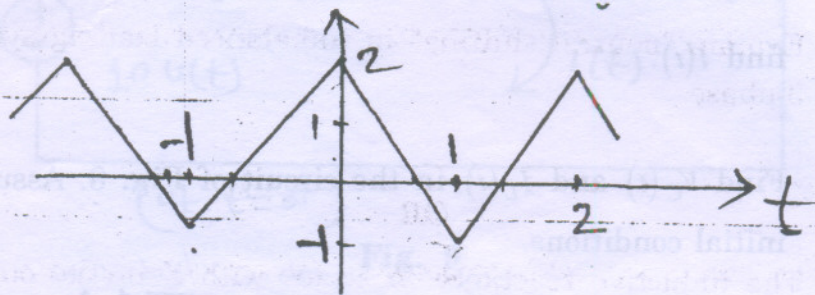


Fig. 6

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- (b) Explain the different kinds of symmetry in non-sinusoidal waves.

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OR

- 4 (a) Derive the expression of power with Non-sinusoidal voltage and current.

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- (b) Obtain the Fourier coefficients of the waveforms shown in Fig. 7.

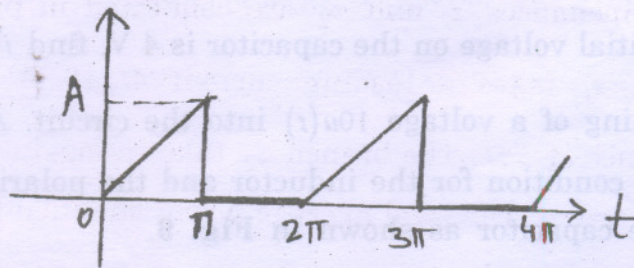


Fig. 7

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UNIT - V

- 5 (a) A ramp voltage $2r(t-z)$ is applied in a series RC circuit at $t=0$ where $R=3\ \Omega$, $C=1\ F$. Assuming zero initial conditions, find $i(t)$.

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- (b) Find $V_C(t)$ and $I_L(t)$ in the circuit of Fig. 8. Assume zero initial conditions.

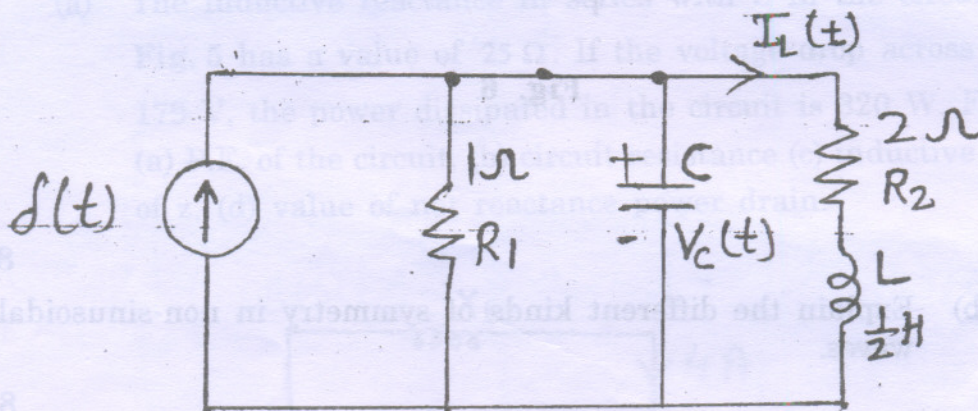


Fig. 8

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OR

- 5 (a) Derive the expression for impulse response of series RL and series RC network by using Laplace transform.

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- (b) In a series RLC network, $R=0.5\ \Omega$, $L=1\ H$ and $C=1\ F$. If the initial voltage on the capacitor is $4\ V$, find $i(t)$ following switching of a voltage $10u(t)$ into the circuit. Assume zero initial condition for the inductor and the polarity of charge on the capacitor as shown in Fig. 9.



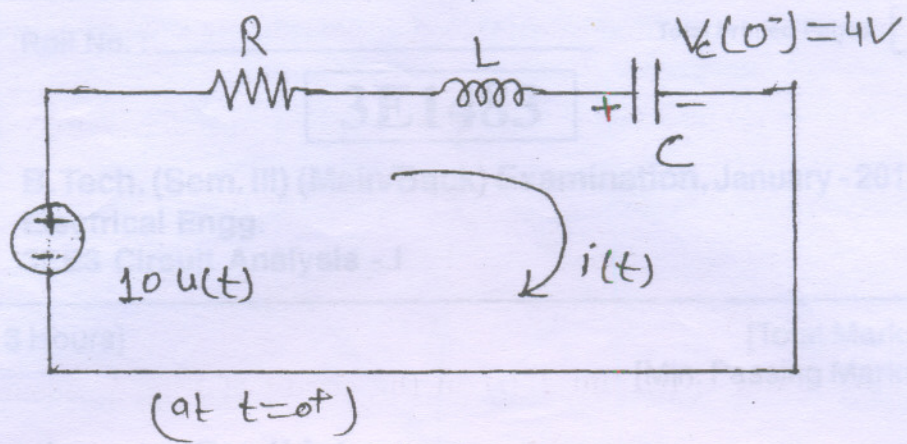


Fig. 9

Instructions to Candidates

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(Mentioned in Part No. 203)

UNIT - I

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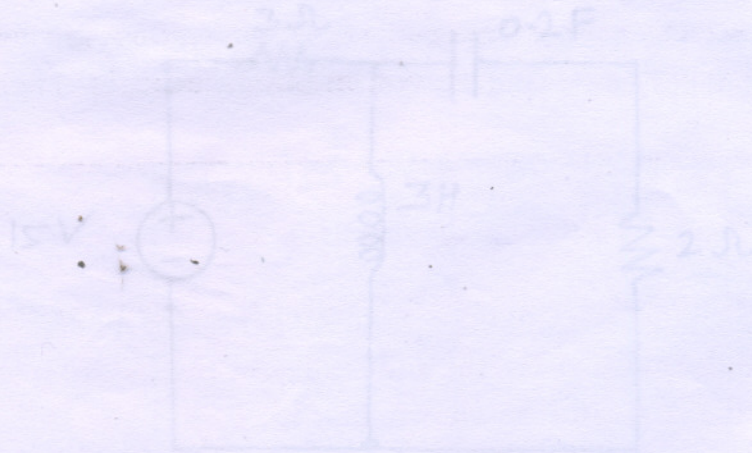


Fig. 1

