8E4093

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B. Tech. (Sem. VIII) (Main/Back) Examination, April/May - 2012
Electronics & Comm.
8EC4.2VHDL (Common with 8EC4.2, 8EX4.2)

Time : 3 Hours] [Total Marks : 80
[Min. Passing Marks : 24

*Attempt any **five questions**, selecting **one question** from **each** unit. **All** questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary.) Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. Nil

UNIT - I

1 (a) What is VHDL ? Explain how variables, signals and constants are declared and used in VHDL. 6

(b) Explain various steps of design flow of ASIC with suitable diagram. 10

OR

2 (a) Briefly explain history of hardware description languages and compare various hardware description languages. 8

(b) Distinguish between :

(i) VHDL IF and VHDL case

(ii) VHDL Next and Exit

(iii) Verilog Repeat and Forever

(iv) Library and Module. 8

UNIT - II

3 (a) Define decoder and implement the function $f(w_1, w_2, w_3) = \Sigma\ (0, 1, 3, 4, 7)$ using 3 to 8 decoder and OR gate. 6

(b) Write VHDL code for a BCD to seven segment converter using selected signal assignment. 10

OR

4 (a) Define multiplexer. How an 16 × 1 MUX can be implemented using two 8 × 1 MUX ? 6

(b) Write VHDL code for 4 bit comparator. 10

UNIT - III

5 (a) Write structural VHDL description for n bit serial-in serial-out shift register. 8

(b) Write a VHDL description for S-R latch

(i) Use a conditional assignment statement

(ii) Use a characteristic equation

(iii) Use two logic gates. 8

OR

6 (a) Write VHDL code to model binary asynchronous 4 bit counter. 10

(b) Write VHDL code for D flip flop. 6

UNIT - IV

7 (a) Derive the state diagram for an FSM that has an input W and output Z. The machine has to generate Z=1, when the previous four values of W were 1001 or 1111 else 0. Overlapping input patterns are not allowed. Write VHDL code for above FSM. 10

(b) Draw block and state diagram of vending machine. 6

OR

8 (a) What are differences between Mealy and Moore type of FSM. 6

(b) Explain Moore type FSM using state diagram, state table and state assigned table. 10

UNIT - V

9 (a) Design a 4-bit binary multiplier and generate the control state graph and table which defines the operation of a binary multiplier. 10

(b) Explain shifting and sorting operations. 6

OR

10 Write short notes on : (any two)

(a) CPU organization

(b) SRAM

(c) Clock synchronization. 8×2=16
