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7E1827

Roll No. _____ Total No. of Pages: 3

7E1827

B. Tech. VII - Sem. (Main / Back) Exam., - 2024
Electronics & Communication Engineering
7EC5-11 Program Elective VLSI Design

Time: 3 Hours **Maximum Marks: 70**

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and three questions out of five questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

[10×2=20]

(Answer should be given up to 25 words only)

All questions are compulsory

Q.1 Define logical effort.

Q.2 What is body effect?

Q.3 State the difference between enhancement and depletion mode MOSFET.

Q.4 Define Elmore delay with necessary equations.

Q.5 Draw transistor level diagram of tri-state inverter and explain it.

Q.6 What is sub threshold conduction? Explain briefly.

Q.7 What is layout optimization using Eular path? Explain briefly.

Q.8 State the difference between SRAM and DRAM.

Q.9 What are the advantages and disadvantages of dynamic logic?

Q.10 What is the difference between ASIC and FPGA?

PART – B

[5×4=20]

(Analytical/Problem solving questions)

Attempt any five questions

Q.1 What is skewed inverter? Explain the beta ratio effect on the CMOS inverter transfer characteristic.

Q.2 The NMOS device with $V_t = 0.7V$ has its source terminal grounded and a 1.3V is applied to gate. The device has $\mu_n C_{ox} = 100$ mA/V^2, W = 10 mm, L = 1mm. Find the value of drain current for $V_{DD} = 3V$.

Q.3 What is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.

Q.4 What is pre charge and evaluation logic? Explain briefly.

Q.5 Why power dissipation is considered as an important factor in CMOS design? Write an expression for different types of power dissipation in CMOS circuits.

Q.6 What is clocked CMOS logic? State its advantages also.

Q.7 What is latch up? How it is avoided in CMOS technology?

PART – C

[3×10=30]

(Descriptive/Analytical/Problem Solving/Design Questions)

Attempt any three questions

Q.1 Draw the MOS transistor circuit model. Give the justification for all capacitances. Compare the different capacitances and explain in detail for overlap capacitance.

Q.2 Give an expression for the output voltage for the pass transistor networks shown in Fig.1. Neglect body effect. Assume V_{tp} and V_{tn} are threshold voltages of PMOS and NMOS transistor respectively.

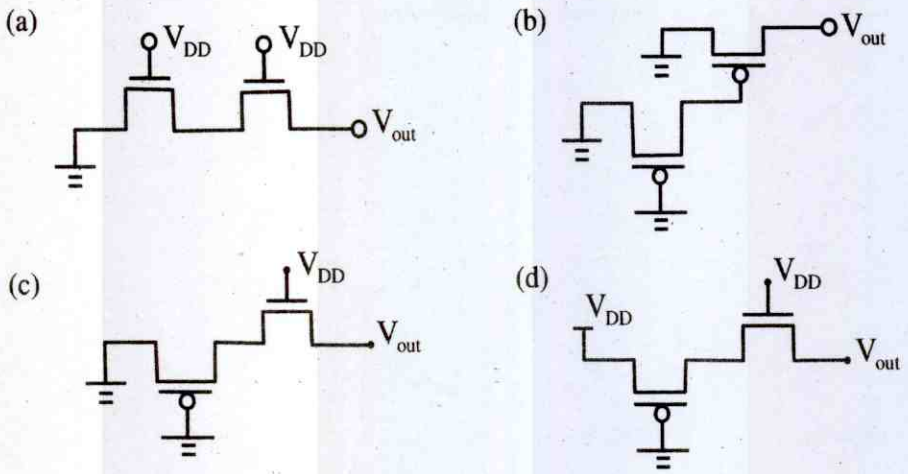

Fig.1

Q.3 Realize the following expression using CMOS -

(i) $AB + \overline{AB}$

(ii) $\overline{A + BC + DE}$

Find W/L for all transistors also.

Q.4 Design $Y = \overline{(AB + CD)}$ using DOMINO logic.

Q.5 Write the VHDL code for following -

(i) JK Flip flop

(ii) 4 : 1 multiplexer

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7E1811

Roll No. _____ Total No. of Pages: 2

7E1811

B. Tech. VII - Sem. (Main / Back) Exam., - 2024

Open Elective – I

7AG6-60.2 Environmental Engineering and Disaster Management

Time: 3 Hours **Maximum Marks: 70**

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and three questions out of five questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

[10×2=20]

(Answer should be given up to 25 words only)

All questions are compulsory

Q.1 What is the importance of safe water supply?

Q.2 What are the standard of drinking water?

Q.3 What is solid waste?

Q.4 What are the different types of pollutions?

Q.5 What is disaster management?

Q.6 What do you mean by wastewater?

Q.7 Define chemical oxygen demand.

Q.8 Define total organic carbon.

Q.9 What are the physical & chemical parameter of the water quality?

Q.10 What are the different types of pollutant in wastewater?

PART – B

[5×4=20]

(Analytical/Problem solving questions)

Attempt any five questions

Q.1 What is hardness? Define Dissolve oxygen and Biological oxygen demand.

Q.2 Why soiling and corrosion are hidden cost of air pollution? Explain.

Q.3 How do individual contaminants affects human health? Explain it.

Q.4 Differentiate between natural and man-made pollution with examples.

Q.5 Discuss the role of green house in disaster management.

Q.6 Explain term Air Pollution. Discuss the types of air pollutants which causes air pollutions.

Q.7 Write the different step involve in domestic wastewater treatment plant.

PART – C

[3×10=30]

(Descriptive/Analytical/Problem Solving/Design Questions)

Attempt any three questions

Q.1 What is landslide? What are the causes of landslide? Explain.

Q.2 Explain term deforestation. Discuss the factors promoting deforestation.

Q.3 Discuss the treatment methods of effluent domestic water, wastewater and industrial wastewater.

Q.4 What are the different BIS standard for pollutants in air? Explain it.

Q.5 Discuss manmade disaster due to lack of public awareness. Explain relationship between national security and disaster.

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7E1729

Roll No. _____ Total No. of Pages: 2

7E1729

B. Tech. VII - Sem. (Re Back) Exam., - 2024
Electronics & Communication Engineering
7EC5-13 CMOS Design

Time: 3 Hours **Maximum Marks: 120**
Min. Passing Marks: 42

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

[10×2=20]

(Answer should be given up to 25 words only)

All questions are compulsory

Q.1 What is Body effect?

Q.2 Why NAND gate is preferred over NOR gate for fabrication?

Q.3 What is Noise Margin?

Q.4 What means by sizing of inverter?

Q.5 What is the difference between testing and verification?

Q.6 Define Latch-Up.

Q.7 Why are all contacts typically of the same size in a CMOS process?

Q.8 Write the advantage of CMOS technology.

Q.9 What are the different layers in MOS Transistors?

Q.10 What is a FPGA?

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PART – B

[5×8=40]

(Analytical/Problem solving questions)

Attempt any five questions

Q.1 Describe Non-ideal behavior of MOS Transistor.

Q.2 Explain the propagation delay and power consumption issues of CMOS gate.

Q.3 Explain and derive the necessary DC region equations of a CMOS inverter.

Q.4 Describe the leakage currents in SRAM cell. Compare the SRAM and DRAM.

Q.5 Write the VHDL Code for S-R Flip-Flop.

Q.6 What are the various issues in CMOS dynamic logic design? Explain anyone with a neat sketch.

Q.7 A digital CMOS IC is operating at 10 MHz clock frequency consumes 100 MW power, the same IC operating at 15 MHz clock frequency consumes 140 MW power, what is the static power consumption of IC?

PART – C

[4×15=60]

(Descriptive/Analytical/Problem Solving/Design Questions)

Attempt any four questions

Q.1 Define Threshold Voltage (V_{TH}). Discuss the dependency of (V_{TH}) on various parameters. Explain the DC noise margin of CMOS logic.

Q.2 Using the example of full adder, explain the structural, behavioral and dataflow style of modeling in VHDL.

Q.3 Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram, also explain the design of CMOS NAND gate.

Q.4 Draw following and explain their working –

(a) NORA Logic (b) DOMINO Logic

Q.5 What type of language is VHDL? Explain advantages and limitations of VHDL Language.

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7E1727

B. Tech. VII - Sem. (Re Back) Exam., - 2024
Electronics & Communication Engineering
7EC5-11 VLSI Design

Time: 3 Hours **Maximum Marks: 120**
Min. Passing Marks: 42

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five questions from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

[10×2=20]

(Answer should be given up to 25 words only)
All questions are compulsory

Q.1 Draw VI characteristics of depletion type MOSFET.
Q.2 Draw the circuit diagram for CMOS two input NOR gate.
Q.3 Write the name of any two technologies used for the fabrication of CMOS transistor.
Q.4 Draw the basic circuit of NMOS and CMOS inverter.
Q.5 What are the advantages and disadvantages of dynamic logic?
Q.6 What is domino CMOS logic?
Q.7 Write the formula for propagation delay for NMOS inverter.
Q.8 What do you understand by pre-charge state?
Q.9 Give an example of data flow style of modelling.
Q.10 Why signals are used in VHDL?

PART – B

[5×8=40]

(Analytical/Problem solving questions)

Attempt any five questions

Q.1 What are the different factors affecting the threshold voltage of MOSFET? Derive the formula used.

Q.2 Derive the V-I characteristics of enhancement MOSFET and explain -
(i) Ohmic region
(ii) Saturation region

Q.3 Draw the CMOS logic circuit for the Boolean expression -
Z = [A(B+C) + DE].

Q.4 Design following using transmission gate -
(i) XOR Gate
(ii) NAND Gate

Q.5 Define "Euler path". And draw stick diagram for NOR gate.

Q.6 Explain the Nora CMOS logic with suitable example.

Q.7 Write VHDL code for full adder in structural style of modelling.

PART – C

[4×15=60]

(Descriptive/Analytical/Problem Solving/Design Questions)

Attempt any four questions

Q.1 Write the layout design rule and draw diagram for four input NAND and NOR gate.

Q.2 What is transistors sizing? Design a Y = ABC logic such that its equivalent (D/L) of pull up section is 90 and pull-down section is 30.

Q.3 Write short note on basic memory circuit and explain SRAM and DRAM in detail.

Q.4 Explain about building block architecture of FPGA.

Q.5 Explain different modelling style used in VHDL, and write VHDL code for SR flip flop using behavioral style of modelling.

7E7081

Roll No. _____ Total No. of Pages: 4

7E7081

B. Tech. VII - Sem. (Old Back) Exam., - 2024
Electronics & Communication Engineering
7EC1A Antennas & Wave Propagation

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Define and explain the following terms of antenna - [8]

(i) Beam-width

(ii) Directivity

(iii) Effective aperture

(iv) Antenna efficiency

(b) What are the roles of an antenna in wireless technology? Explain how the concept of displacement current was introduced by Maxwell's to account for the production of magnetic fields in free space. [8]

OR

Q.1 (a) With the help of Maxwell's equation, explain how radian and reception of EM wave takes place? Isotropic radiator is only a theoretical concept; it cannot be designed practically, why? [8]

(b) An antenna has normalized radiation intensity $U(\theta, \phi) = 10 \sin\theta \sin\phi$; W/sr for $0 < \theta < \pi$ and $0 < \phi < 2\pi$ and zero elsewhere. Find the radiated power and directivity. [8]

UNIT- II

Q.2 What is phased array antenna? What is the main difference between BSA and EFA? Plot the normalized field pattern for BSA and EFA by considering an array of eight elements spaced at $\lambda/2$. [16]

OR

Q.2 Define the principle of pattern multiplication of an antenna array. A uniform linear array consists of 14 isotropic point sources with spacing of $\lambda/4$, Calculate - [16]

(i) Directivity

(ii) Effective aperture, if the phase difference $\delta = -90°$

UNIT- III

Q.3 (a) Design a three-element Yagi-Uda antenna to operate at a frequency of 570 MHz. [6]

(b) What are the different categories of lens antennas? Explain the basic principle of operation of a dielectric lens antenna, showing how it converts a spherical wave front into a plane wave front. Also, derive the lens equation. [10]

OR

Q.3 (a) Calculate the design data of a rhombic antenna to operate at 50 MHz, if the angle of elevation is 30°. [6]

(b) Design a rectangular micro-strip patch with dimensions W and L over a single substrate, whose center frequency is 10 GHz. The dielectric constant of the substrate is 10.2 and the height of the substrate is 0.127 cm. Determine the physical dimensions W and L (in cm) of the patch, taking into account field fringing. [10]

UNIT- IV

Q.4 (a) Explain the formation of ionosphere. What are the various layers of the ionosphere and their effects on wave propagation? With the help of a neat diagram show their height of the ground. [8]

(b) Explain with suitable diagram "the multiple hope transmission". Also describe the effect of earth's magnetic field on ionosphere wave propagation. [8]

OR

Q.4 (a) What do you understand by duct propagation? Under what condition are ducts formed? Discuss the frequency bands useful for duct propagation. What are its main limitations? [8]

(b) What is tropospheric scattering? What is the frequency range for it? What are the major conditions for its operation? [8]

UNIT- V

Q.5 (a) Define the critical frequency and critical angle. How critical frequency and critical angle related with electron density? [4]

(b) What are the effects of ground on antennas? Also, describe the effect of earth's magnetic field on ionosphere wave propagation. [4]

(c) A communication system is to be established at a frequency of 60 MHz with a transmitter power of 2kW. The field strength of the directive antenna is 5 times that of a half-wave antenna, h_t = 60 mm, h_r = 6 m. Field strength of 100 μV/m is required to give satisfactory reception. Find the range of the system. [8]

OR

Q.5 (a) What is meant by fading? Also define skip distance and give the reasons why it varies? [4]

(b) Find the critical frequency if the maximum electron density is 1.3×10^6 electron/cm^3. Also calculate the critical angle of propagation for D-layers, if the transmitter and receiver are separated by 450 km. [4]

(c) A high frequency radio link has to be established between two points at a distance of 2500 km on earth's surface. Considering the ionosphere height to be 200 km and its critical frequency 5MHz, calculate the Maximum Usable Frequency (MUF) for the given path. [8]

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7E7072

Roll No. _____ Total No. of Pages: 3

7E7072

B. Tech. VII - Sem. (Old Back) Exam., - 2024
Applied Electronics & Instrumentation Engineering
7AI2 Digital Signal Processing
AI, EC, EIC

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 Consider the system given in Figure 1. Assume that $H(e^{j\omega})$ is an LTI discrete – time system, $X_C(j\Omega)$ is band limited and sampling rate is above the Nyquist rate. [16]

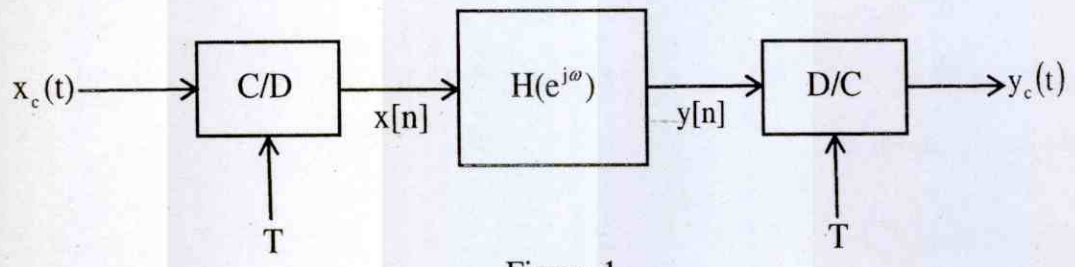

Figure 1

Establish the relationship between $X_C(j\Omega)$ and $Y_C(j\Omega)$.

OR

Q.1 Explain the general system for sampling rate reduction by a factor of M. Obtain a frequency domain relation between the input and output of this system (decimator). [16]

UNIT- II

Q.2 A causal LTI discrete – time system has a system function [16]

$$H(z) = \frac{(1-.07z^{-1})(1-j2z^{-1})(1+j2z^{-1})}{(1-0.8z^{-1})(1+0.8z^{-1})}$$

Find a minimum phase system function $H_{min}(z)$ and a linear phase system function $H_{lp}(z)$ such that $H(z) = H_{min}(z)H_{lp}(z)$. Justify.

OR

Q.2 Discuss the locations and constraints on the zeros for FIR linear – phase systems. [16]

UNIT- III

Q.3 Consider the causal LTI filter with system function [16]

$$H(z) = \frac{1-\frac{1}{5z^{-1}}}{\left(1-\frac{1}{2z^{-1}}+\frac{1}{3z^{-2}}\right)\left(1+\frac{1}{4z^{-1}}\right)}$$

Draw the structure using cascade connection of first and second order systems realized in direct form II.

OR

Q.3 Draw the direct form structures for FIR linear phase systems for type I (even order) and type II (odd order) systems. [16]

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UNIT- IV

Q.4 Design a Butterworth IIR digital filter using bilinear transformation that satisfies the following specifications. [16]

$$0.8 \leq |H(e^{j\omega})| \leq 1.0, \quad 0 \leq \omega \leq 0.2\pi$$
$$|H(e^{j\omega})| \leq 0.2, \quad 0.6\pi \leq \omega \leq \pi$$

OR

Q.4 Using a rectangular window, design an FIR filter with a frequency response

$$H_d(e^{j\omega}) = \begin{cases} 1, & -\frac{\pi}{4} \leq |\omega| \leq \frac{\pi}{4} \\ 0, & \frac{\pi}{4} \leq |\omega| \leq \pi \end{cases}$$

Find h[n] and H(z) for M = 11. [16]

UNIT- V

Q.5 State and prove the circular convolution property of the DFT. [16]

OR

Q.5 Derive and construct a flow graph for a 8 – point radix – 2 decimation – in – time FFT algorithm. Label all multipliers in terms of powers of W_8, and also label any branch transmittances that are equal to – 1. Draw and explain the flow graph of basic butterfly computation used in the above flow graph. [16]

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7E7078

Roll No. _____ Total No. of Pages: 2

7E7078

B. Tech. VII - Sem. (Old Back) Exam., - 2024
Electronic Instrumentation & Control Engineering
7EI3A Digital Image Processing
EC, EIC

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the basic concepts in sampling and quantization digital image processing. [8]

(b) Discuss working of image acquisition system by using CCD sensors. [8]

OR

Q.1 What is Colour model and Colour system? Explain RGB and HSI colour model. [16]

UNIT- II

Q.2 Describes the various types of frequency domain filters. [16]

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OR

Q.2 (a) What is Image Sharpening? Explain first and second order derivatives of image sharpening. [10]

(b) Explain Histogram equalization of an image. [6]

UNIT- III

Q.3 What is digital image restoration process? Explain noise probability density function. [16]

OR

Q.3 Write a short note on -

(a) Inverse filtering [8]

(b) Weiner filtering [8]

UNIT- IV

Q.4 (a) What is Thinning and Pruning? Explain briefly. [8]

(b) Discuss image opening morphological operation by writing its mathematical operation. [8]

OR

Q.4 (a) Explain Erosion and Dilation. [8]

(b) Discuss image closing morphological operation by writing its mathematical operation. [8]

UNIT- V

Q.5 Explain the fundamental of edge-based segmentation. [16]

OR

Q.5 (a) Discuss watershed transform along with it suitable application. [8]

(b) What do you mean by Image Thresholding? [8]
