7E1727

Roll No. _____ [Total No. of Pages : 2

# 7E1727

## B.Tech. VII Sem. (Main&Back) Examination, January - 2023
## Electronics and Comm. Engg.
## 7EC5-11 VLSI Design

**Time : 3 Hours** **Maximum Marks : 120**

**Min. Passing Marks : 42**

***Instructions to Candidates:***

*Attempt **All Ten** questions from **Part A**, **Five** questions out of **Seven** from **Part B** and **Four** questions out of **Five** from **Part C**.*

*Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No.205)*

### PART - A
**(Answer should be given up to 25 words only)**

**All questions are compulsory.** **(10×2=20)**

1. Write region of operations and necessary condition for the MOSFET to works as a resistor and current source.
2. What are the different factors affecting the threshold voltage of MOSFET.
3. Sketch pre - charge and Evaluation logic circuit.
4. What is Latchup problem define? Name methods used to reduce it.
5. What is Subthreshold Leakage in MOS.
6. Draw FPGA/VHDL based ASIC design flow graph.
7. Define via and contacts in layout.
8. Depict the layout design rules for
   i. Well size
   ii. Poly extension.
9. State the reason, why minimum poly extension is required.
10. Draw MOS circuit and layout of multiplexer.

### PART - B
**(Analytical/Problem solving questions)**

**Attempt any Five questions.** **(5×8=40)**

1. Draw and explain the steps of CMOS fabrication.
2. Draw MOS transistor circuit model and explain the origination of each parameter.

3. Sketch Euler path, static CMOS gate implementation and layout with minimum transistors for computing Y' = (A+B).(C+D).

4. Sketch and describe logic circuit realized using.

   i. Domino logic.

   ii. NORA logic.

5. Draw 6T SRAM cell and explain its read write operation.

6. Write the names of three types of power dissipation in CMOS logic circuits and drive the expression for total power dissipation.

7. Draw the layout of XOR gate depicting all the design rule parameter values.

## PART - C

**(Descriptive/Analytical/Problem Solving/Design questions)**

**Attempt any Four questions.** **(4×15=60)**

1. Draw and write the working of depletion mode PMOS with the help of input - output and transfer characteristics. Explain how it can also be used in enhancement mode with depletion mode.

2. Drive the expression for rise time ($t_r$) and fall time ($t_f$) for CMOS inverter.

3. Drive the formula and explain the following in MOS

   i. Body effect and Body effect parameter.

   ii. Channel length modulation and short channel effect.

4. Draw Voltage transfer characteristics (VTC) of CMOS inverter and drive the expression for Bn/Bp ratio.

5. Write VHDL code for

   i. J-K flip - flop.

   ii. 3 - input NAND gate.

621

7E1729

Roll No. _____ [Total No. of Pages : 3

# 7E1729

## B.Tech. VII - Sem. (Main/Back) Examination, January - 2023
## Electronics and Comm. Engg.
## 7EC5-13 : CMOS Design

**Time : 3 Hours** **Maximum Marks : 120**
**Min. Passing Marks : 42**

***Instructions to Candidates:***

*Attempt all **Ten** questions from Part A. **Five** questions out of **Seven** from Part B and **Four** questions out of **Five** from Part C.*

*Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be sated clearly.*

*Use of following supporting materials is permitted during examination. (Mentioned in form No.205)*

**PART - A**

**(Answer should be given up to 25 words only)**

**All questions are compulsory.** **(10×2=20)**

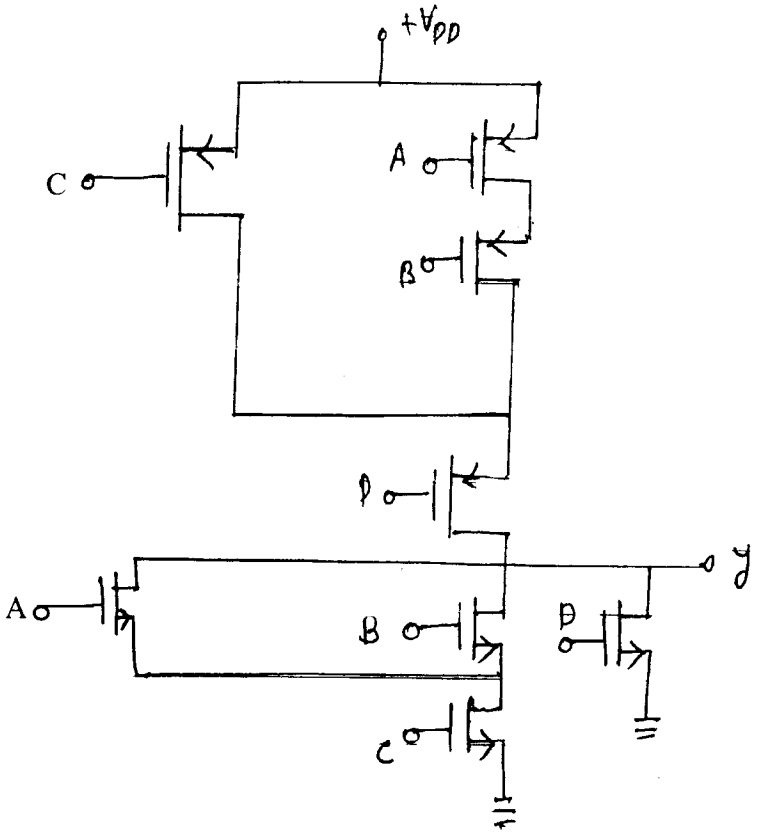
1. Define Entity.
2. What is behavioural model?
3. What is resolution function?
4. What are the various sources of power dissipation in CMOS circuits?
5. What are test benches.
6. Why is NAND gate preferred over NOR gate for fabrication.
7. Write the characteristics of CMOS logic families.
8. In a 2-input CMOS logic gate, one input is left. Floating i.e., connected neither to ground nor to a signal. What will be the state of that input?
9. Define Accumulation Phenomenon in MOS structure.
10. What is Body Effect?

## PART - B

### (Analytical/Problem solving questions)

**Attempt any Five questions.** **(5×8=40)**

1. The CMOS circuit shown below implements the function




2. A digital CMOS IC operating at 10MHz clock frequency consumes 100mw power, the same IC operating at 15mHz clock frequency consumes 140 mw power. What is the static power consumption of the IC.

3. Design a 3 - Input NAND gate using CMOS such that its pull up to pull down ratio of equivalent size is 3.

4. Draw stick diagram layout for :

   i) 2 - Input CMOS NAND gate.

   ii) Ex-OR gate.

5. What is $C^2$ MOS logic? Draw any logic circuit using it. What are additional advantages of such logic.

6. Write the difference between custom design and FPGA in respect of design time and cost.

7. Explain NORA CMOS logic circuit in details.

## PART - C

**(Descriptive/Analytical/Problem Solving/Design questions)**

**Attempt any Four questions.** **(4×15=60)**

1. Draw following and explain their working.

   i) SRAM and DRAM cell.

   ii) $y=\left(\overline{AB+C}\right)$ using domino logic.

   iii) Any NP (Zipper) logic.

2. Using the example of full adder, Compare and contrast the data flow, behavioural and structural style of modeling in VHDL.

3. Draw the CMOS inverter and discuss its DC characteristics. Write the condition for different regions of operation.

4. What type of language is VHDL? Explain advantages and limitation of VHDL language.

5. Draw the following Circuits

   i) $y=A\bar{B}C$ using CMOS.

   ii) 1 bit memory cell using CMOS.

   iii) $y=A\oplus B$ using transmission gate.

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7E1723

Roll No. _____ [Total No. of Pages : 2

# 7E1723

## B.Tech. VII - Sem. (Main / Back) Examination, January - 2023
## Open Elective-I
## 7CS6-60.2 Cyber Security

**Time : 3 Hours** **Maximum Marks : 120**
**Min. Passing Marks : 42**

***Instructions to Candidates:***

***Attempt All Ten questions From Part A, five questions out of seven questions from Part B and four questions out of five questions from Part C .***

*Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No.205)*

## PART - A

**(Answer should be given up to 25 words only)**

**All questions are compulsory.** **(10×2=20)**

1. What is cyber stalking?
2. Explain phishing attack.
3. Explain E-mail spoofing.
4. What is spamming?
5. What are the advantages of cloud computing?
6. What is the use of firewall?
7. What is digital signature?
8. Explain types of firewall.
9. What is steganography?
10. Explain Spywares.

## PART - B

### (Analytical/Problem solving questions)

**Attempt any Five questions.** **(5×8=40)**

1. Differentiate between virus and worms.
2. What are cybercrimes? Explain the classification of cybercrime.
3. How criminals plan the attacks on social media and financial sites.
4. What is Trojan Horse? Explain its attack in detail.
5. Explain security implications for organizations.
6. Discuss cybercrime in legal perspective and Indian ITA 2000.
7. What are registry settings for mobile devices?

## PART - C

### (Descriptive/Analytical/Problem Solving/Design questions)

**Attempt any Four questions.** **(4×15=60)**

1. What is software piracy? Discuss crime related IPR issues.
2. Discuss management perspective of Cyber security (ISO 27001).
3. Differentiate between DoS and DDos attacks. Also explain security challenges posed by mobile devices.
4. Explain the concept of Virtual Private Network.
5. Explain the following:
   a) SQL injection
   b) Digital forensics.

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7E1731

Roll No. _____ [Total No. of Pages : 2

# 7E1731

## B.Tech. VII-Sem. (Main/Back) Examination, January - 2023
## Open Elective - I
## 7EC6-60.2 Micro and Smart System Technology

**Time : 3 Hours** **Maximum Marks : 120**
**Min. Passing Marks : 42**

***Instructions to Candidates:***

*Attempt all **Ten** questions from **Part A**. **Five** questions out of **seven** from **Part B** and **Four** questions out of **five** questions from **Part C**.*
*Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*
*Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

### PART - A

**(Answer should be given up to 25 words only)**

**ALL TEN questions are compulsory.** **(10×2=20)**

1. What is Miniaturization? Give the name of Miniaturization approaches.
2. Write the applications of MEMS.
3. Give the definition for Smart Materials.
4. What is the need for Smart Systems?
5. Classify the Smart Structures.
6. Why electrostatic actuators are more popular?
7. Write the applications of smart systems.
8. Compare wet etching and dry etching method.
9. What is Low Temperature Cofired Ceramic (LTCC) multi chip module technology.
10. What is the principle of silicon capacitive accelerometer?

522

## PART - B

### (Analytical/Problem Solving Questions)

**Attempt any Five questions.** **(5×8=40)**

1. Draw a block diagram of Smart system and explain the each block in brief.
2. Write a short note on smart materials used in smart systems.
3. What is the need for miniaturization of micro actuators? Discuss the portable clinical analyzer as a example of Microsystems.
4. Discuss the selection of packaging materials for MEMS and Microsystems.
5. Explain the failure mechanisms in Microsystems and testing for reliability of MEMS and Microsystems.
6. Discuss the wire and ball bonding methods of packaging of Microelectronic devices.
7. Write a short note on packaging of micromachined accelerometer or a thermal cycler BEL pressure sensor.

## PART - C

### (Descriptive/Analytical/Problem Solving/Design Questions)

**Attempt any Four questions.** **(4×15=60)**

1. How we can classify the sensors? Discuss the basic characteristics of the sensors. Explain conductometric gas sensors and piezoresistive sensors in detail.
2. Draw a basic diagram of microactuator and explain its characteristics and function. Discuss the Electro thermal and piezoelectric micro actuators with suitable diagrams.
3. Draw a flow chart for fabrication of Microsystems and discuss the thin film deposition methods. What are the parameters to check the quality of thin films?
4. Explain the process of pattern transfer and compare the surface and bulk micromachining process used in fabrications of micro manufacturing. Show the stiction is the major failure mechanism in surface micromachining. How stiction can be minimized?
5. Discuss the scaling issues in miniaturization of microsystems. Explain the processing of the modeling of magnetostrictive actuators and Capillary electrophoresis.

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7E7081

Roll No. _____ [Total No. of Pages : 2

# 7E7081

## B.Tech. VII - Sem. (Back) Examination, January - 2023
## Electronics and Communication Engg.
## 7EC1A : Antenna and Wave Propagation

**Time : 3 Hours** **Maximum Marks : 80**

**Min. Passing Marks : 26**

***Instructions to Candidates:***

*Attempt any **five** questions, selecting **one** question from **each unit**. All questions carry **equal** marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.) Units of quantities used/calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No. 205)*

### UNIT - I

1. Explain the following. **(4×4=16)**
   a. Beamwidth.
   b. Directivity.
   c. Radiation resistance.
   d. Polarization.

**(OR)**

1. a. Explain Reciprocity theorem, explain it for two antenna. **(6)**
   b. Find the expression of radiated power by Half wave dipole antenna. **(10)**

### UNIT - II

2. a. Define pattern multiplication. Using suitable example explain principal of pattern multiplication. **(8)**
   b. Explain the working principal Array of two isotropic point sources. **(8)**

**(OR)**

2. a. Explain the working principal of N-element linear array of elementry dipole. **(8)**
   b. Explain 4-element broadside and end fire arrays. **(8)**

### UNIT - III

3. a. Explain the method of Antenna directivity measurement. **(8)**
   b. Explain the need of patch - antenna. Explain the working of two - element microstrip path antenna. **(8)**

**(OR)**

3. Explain the following :
   a. Folded dipole antenna.
   b. Parabolic reflector Antenna.
   c. Rhombic Antenna.
   d. Log - periodic dipole antenna. **(4×4=16)**

**UNIT - IV**

4. a. Explain the Tropospheric propagation using suitable schematic. **(8)**
   b. Explain the theory of ground reflection. **(4)**
   c. Compare space and surface wave. **(4)**

**(OR)**

4. Explain the following.
   a. Vertical polarization.
   b. Tropospheric propagation.
   c. Duct propagation. **(5+5+6=16)**

**UNIT - V**

5. a. Explain different electrical properties of ionosphere and their effects on wave propagation. **(8)**
   b. Explain virtual height. Derive expression for maximum usable frequency. **(8)**

**(OR)**

5. Explain the following.
   a. Various ionospheric layers.
   b. Multiple hop transmission.
   c. Effect of earth's magnetic field. **(5+5+6=16)**

7E7072

Roll No. _____ [Total No. of Pages : 2

# 7E7072

## B.Tech. VII-Sem. (Back) Examination, January - 2023
## Applied Electronics and Instrumentation Engg.
## 7AI2 : Digital Signal Processing
## AI, EC, EIC

**Time : 3 Hours** **Maximum Marks : 80**

**Min. Passing Marks : 26**

***Instructions to Candidates:***

*Attempt any **five** questions, selecting **one** question from **each** unit. **All** questions carry **equal** marks. (Schematic **diagrams** must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.)*

*Use of following supporting material is permitted during examination. (Mentioned in form No.205)*

### UNIT - I

**1.** a) Explain the discrete time processing of continuous time signal by drawing the neat block diagram and writing the appropriate mathematical expressions. **(8)**

b) Explain:

i) Decimator. **(4)**

ii) Interpolator. **(4)**

**(OR)**

**1.** a) Explain the methods of changing the sampling rate. **(8)**

b) Explain the importance of sampling theorem. **(8)**

### UNIT - II

**2.** Explain the following with the examples.

a) Minimum phase system. **(8)**

b) Linear system with linear phase. **(8)**

**(OR)**

**2.** a) Prove that the group delay of first order all pass system is given as

$$\tau^2(w) = \frac{1-r^2}{\left|1 - r\, e^{j\theta}\, e^{-jw}\right|^2}$$ **(8)**

b) Explain the followings:

i) Symmetric property of LTI system.

ii) Magnitude and phase response of LTI system. **(8)**

## UNIT - III

3. Derive the expression of $H(z)$ for linear phase symmetric FIR filter for following case
   a) M odd (8)
   b) M even. (8)

**(OR)**

3. Explain the followings:
   a) Frequency sampling FIR structure. (8)
   b) Lattice structure of IIR filter (8)

## UNIT - IV

4. a) Describe the desirable features of the window function and the effect of windowing. (8)
   b) Compare between the frequency domain characteristics of rectangular, hamming and hanning window. (8)

**(OR)**

4. a) What is the frequency warping effect? What is the cause of this effect. (8)
   b) Write down the steps to design the IIR butterworth filter. (8)

## UNIT - V

5. a) Differentiate CTFT, DTFT and DFT with the neat diagram. (8)
   b) Explain all the properties of DFT. (8)

**(OR)**

5. Explain the decimation in time FFT algorithm in details. (16)

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7E17078

Roll No. _____ [Total No. of Pages : 3

7E7078

# B.Tech. VII - Sem. (Back) Examination, January - 2023
## Electronic Instrumentation & Control Engineering
## 7EI3A Digital Image Processing
## EC, EIC

**Time : 3 Hours** **Maximum Marks : 80**

**Min. Passing Marks : 26**

***Instructions to Candidates:***

*Attempt any **Five questions**, selecting **One question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitable to be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No.205)*

### UNIT - I

1. What is the benefit of using different color models in digital images? Write abou the RGB and HSI color models briefly and state about their transformation formulation. **(16)**

**(OR)**

1. Discuss digital image acquisition process using CMOS sensors. Compare it with CCD image sensors. **(16)**

### UNIT - II

2. Apply histogram equalization for enhancing the following 3-bit image. **(16)**

| | | | | |
|---|---|---|---|---|
| 1 | 0 | 2 | 1 | 0 |
| 3 | 0 | 2 | 2 | 1 |
| 3 | 1 | 3 | 2 | 3 |
| 2 | 2 | 1 | 2 | 1 |

**(OR)**

2. Given 3×5 underexposed 8-bit image is enhanced by 'Gamma correction' tecnique (with $\gamma = 0.85$). Calculate the modified image pixel intensity levels at the bold marked pixels.

| | | | | |
|---|---|---|---|---|
| 125 | 49 | 77 | 62 | 77 |
| 97 | **52** | **107** | **47** | 68 |
| 117 | 67 | 52 | 40 | 127 |

**(16)**

## UNIT - III

3. Apply 3×3 mean filtering on the following image at the bold marked pixels. **(16)**

| | | | | |
|---|---|---|---|---|
| 19 | 22 | 33 | 20 | 32 |
| 34 | **250** | **218** | **201** | 26 |
| 49 | 67 | 0 | 79 | 52 |

**(OR)**

3. Apply 3×3 median filter on the bold marked pixels to minimize the salt-and-pepper noise. **(16)**

| | | | | | |
|---|---|---|---|---|---|
| 19 | 22 | 33 | 20 | 32 | 54 |
| 77 | **255** | **0** | **0** | 26 | 78 |
| 49 | 67 | 75 | 39 | 99 | 110 |

## UNIT - IV

4. For the given 8×6 image, apply the image erosion process by using the structuring element as shown below: **(16)**

| | | | | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| 1 | 1 | 1 |

**(OR)**

4. Discuss image erosion and dilation process by writing their mathematical expressions and explain the operation by taking a suitable example for each of the two. **(16)**

## UNIT - V

5. Apply the Laplacian operator for calculating the edge map at the bold pixel positions in the following image: **(16)**

| | | | | |
|---|---|---|---|---|
| 27 | 37 | 66 | 43 | 39 |
| 43 | 210 | 139 | 159 | 117 |
| 78 | **55** | **31** | **78** | 63 |
| 134 | 188 | 198 | 178 | 119 |
| 110 | 99 | 88 | 106 | 97 |

**(OR)**

5. Discuss the following:

a) Edge detection by using Sobel mask

b) Watershed transformation

c) Lossless versus lossy compression.

**(5+5+6=16)**

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7E7084

Roll No. _____ [Total No. of Pages : 2

# 7E7084

## B.Tech. VII - Sem. (Back) Examination , January - 2023
## Electronics and Communication Engg.
## 7EC5A VLSI Design

**Time : 3 Hours** **Maximum Marks : 80**
**Min. Passing Marks : 26**

***Instructions to Candidates:***

*Attempt any **five** questions, selecting **one** question from **each unit**. **All** questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

*Use of following supporting material is permitted during examination. (Mentioned in form No.205)*

### UNIT - I

1. a. Explain the NMOS Fabrication process in detail. **(8)**

   b. Discuss following High order effects in MOSFET.

      i. Narrow channel effect **(4)**

      ii. Punch through effect **(4)**

**(OR)**

1. a. What are different kinds of MOS transistors? Explain the structure and operation of MOS transistor. **(8)**

   b. Draw and write the working of enhancement mode PMOS with the help of input output and transfer characteristics. **(8)**

### UNIT - II

2. a. Determine the pull up to pull down ratio $(Z_{Pu} / Z_{Pd})$ for a NMOS inverter driven by another NMOS inverter. **(8)**

   b. Write the names of three types of power dissipation in CMOS logic circuits and derive the expression for total power dissipation. **(8)**

**(OR)**

2. a. Draw and explain the working of Transmission Gate (TG). Use it for the 2X1 CMOS multiplexer. **(8)**

   b. What is noise margin? Explain the procedure to determine noise margin. **(8)**

## UNIT - III

3. a. What is Latch up Problem? How it can be avoided in CMOS circuits? **(8)**

   b. What are DRC rules for layout? State any six DRC rules. **(8)**

**(OR)**

3. a. Explain the layout for NAND with suitable example. **(8)**

   b. Draw the Layout for a Half Adder using CMOS logic. **(8)**

## UNIT - IV

4. Draw and explain any **Two** logic circuits from the following : **(2×8=16)**

   i. Clocked CMOS logic

   ii. SRAM

   iii. NP (ZIPPER) logic

   iv. PE (Pre - charge and Evaluation) logic

## UNIT - V

5. a. Write VHDL Code for S-R flip flop and D flip flop. **(10)**

   b. List the advantages and limitations of VHDL. **(6)**

**(OR)**

5. a. Explain the ECAD tools for first and back end design. **(8)**

   b. Write VHDL Code for 2 input NAND and NOR gate. **(8)**

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