(L) 459

7E1727

Roll No. _____ Total No. of Pages: 4

7E1727

B. Tech. VII - Sem. (Main / Back) Exam., January - 2022
Electronics & Communication Engineering
7EC5 –11 VLSI Design

Time: 3 Hours **Maximum Marks: 120**
Min. Passing Marks: 42

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Draw the circuit diagram of SRAM.

Q.2 What is VHDL?

Q.3 Explain "Twin-tub CMOS fabrication.

Q.4 Write the VHDL code of 2×1 multiplexer.

Q.5 What is Body effect?

Q.6 Differentiate between Fan in and Fan out.

Q.7 Draw the energy band diagram of ideal MOS structure.

Q.8 Briefly explain the FPGA circuits.

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Q.9 Compare depletion and enhancement mode transistor actions.

Q.10 Discuss MOS transistor oxide and junction capacitors variation with scaling and biasing.

PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 Write the short note on ECAD tools for front and back end design of VLSI circuits.

Q.2 Briefly explain with schematic (i) Domino logic (ii) NORA logic (iii) NP(ZIPPER) Logic, PE (pre-charge) logic (iv) Clocked CMOS (C^2MOS) logic.

Q.3 What is MOS capacitor? Draw its CV diagram at Low frequency and High frequency.

Q.4 Write the VHDL code of Universal Shift registers.

Q.5 Draw the structure of depletion mode transistor. Also draw the fabrication steps.

Q.6 Draw the layout diagram for –

(a) 2 – input CMOS NAND gate

(b) 2 – input CMOS NOR gate

Q.7 Derive an expression for pull up to pull down ratio for a CMOS inverter.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 Two logic functions given by F =A + B + C and G = A + B + C + D. Assume both true and complementary signals are available.

(a) Implement these functions in dynamic CMOS as cascaded ϕ stages so as to minimize the total transistor count.

(b) Discuss any conditions under which this implementation would fail to operate properly.

(c) Design an np – CMOS implementation of the same logic functions. Does this design display any of the difficulties of part (b)?

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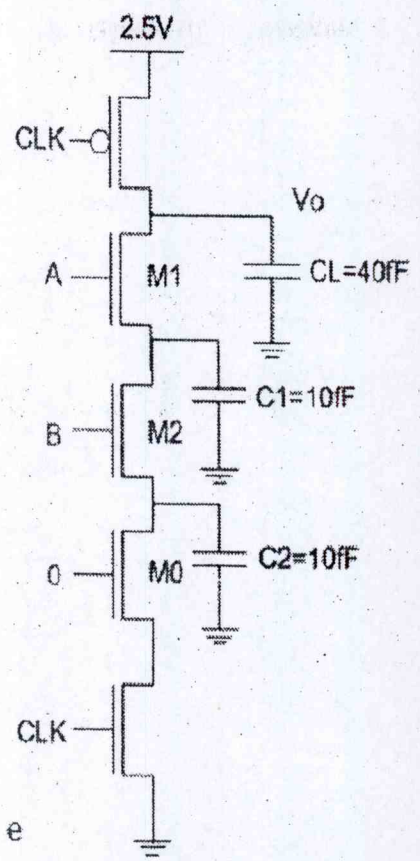
Q.2 Give the following circuit, assuming that all inputs of the circuit shown in Figure below are initially 0 during the pre-charge phase and that all internal nodes are at 0V,



(a) Calculate the voltage drop on Vo, if a changes to 1 (V_{DD} = 2.5V) during the evaluate phase. It is given that V_{tn0} = 0.5V, $2\varphi_F$ = 0.6V and $\gamma = 0.4V^{0.5}$. Hint: Don't forget the body effect.

(b) Now calculate the voltage drop on Vo if both A and B change to 1 (under the above conditions).

(c) What is the maximum number of transistors that can be connected in series to M1 and M2 (including M1 and M2, excluding M0) if the output should not fall below 0.9V during the evaluate phase? Assume that each one of the new transistors has the same intrinsic capacitance (to ground) as M1 and M2 (C = 10fF).

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Q.3 What is MOS capacitor? Draw its CV diagram at Low frequency and High frequency. Define Noise margin and Transistor Trans-conductance g_m.

Q.4 Explain the different types of layout design rules and compare them with application. Discuss the following –

(a) Layout issues for inverter

(b) Layout optimization for performance.

Q.5 Explain power dissipations in the CMOS logic circuits. Draw two input multiplexer using transmission gate.

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7E1729

Roll No. _____ Total No. of Pages: 2

7E1729

B. Tech. VII - Sem. (Main / Back) Exam., January - 2022
Electronics & Communication Engineering
7EC5 –13 CMOS Design

Time: 3 Hours **Maximum Marks: 120**
Min. Passing Marks: 42

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Define the short channel devices.
Q.2 What is stick diagram? What are the uses of stick, diagram?
Q.3 What is the channel length modulation?
Q.4 How to minimize the dynamic power dissipation?
Q.5 Write the features of CMOS domino logic.
Q.6 Differentiate between channeled and channel less gate array.
Q.7 Mention the levels at which testing of a chip can be done.
Q.8 How data path can be implemented in VLSI?
Q.9 Define clock skew and clock jitter.
Q.10 Differentiate between latches and flip-flop.

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PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 Explain the operation of PMOS enhancement transistor with a suitable diagram.

Q.2 Explain the transmission gate and the tri-state inverter with a suitable diagram and operation.

Q.3 Explain the multiplexers and latches using transmission gate with a suitable diagram.

Q.4 Explain the concept of MOSFET as switches and also bring the various logic gates using the switching concept.

Q.5 Explain the followings –

(i) DOMINO Logic

(ii) NORA Logic

Q.6 Explain the latch up prevention techniques.

Q.7 Explain the followings regarding the CAD tools –

(i) Layout editors

(ii) Design Rule Checkers (DRC)

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 Derive the CMOS inverter DC characteristics and obtain the relationship for output voltage at different region in the transfer characteristics.

Q.2 Explain the various CMOS fabrication technology with suitable diagrams.

Q.3 Explain the concept involved in structural gate level modelling and give the description for Half Adder and Full Adder.

Q.4 Explain the ASIC, design flow with a neat diagram.

Q.5 What is ASIC? Explain the types of ASIC in detail.

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7E1730

Roll No. _____ Total No. of Pages: 2

7E1730

B. Tech. VII - Sem. (Main / Back) Exam., March - 2022

Open Elective - I

7EC6 – 60.1 Principle of Electronic Communication

Time: 3 Hours **Maximum Marks: 120**

Min. Passing Marks: 42

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) [10×2=20]

All questions are compulsory

Q.1 Define modulation index and percentage modulation for an AM wave.

Q.2 Distinguish between low level and high level modulation.

Q.3 Define the image frequency.

Q.4 Differentiate between GSM and CDMA telecommunication.

Q.5 What is the need of CPG message in ISUP protocol?

Q.6 What is MTO?

Q.7 How the signal is amplified in fiber optic cable?

Q.8 Give the 3 – different types of application with respect to satellite system.

Q.9 What is meant by DOM set?

Q.10 Mention the three regions to allocate the frequency for satellite services.

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PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 Compare PAM, PWM and PPM.

Q.2 Derive an expression of quantization error (in terms of power) for linear quantization.

Q.3 Give the comparison of Pulse code modulation, Delta modulation, Adaptive delta modulation and Differential pulse code modulation.

Q.4 Derive the expression of error probability of BPSK signal employing coherent reception.

Q.5 Explain the Altitude and Orbit Control System (AOCS) regarding satellite subsystems.

Q.6 Draw the block diagram of optical fiber communication system and explain it.

Q.7 Explain the frequency reuse concept in wireless communication.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 Explain in detail how can we improve the coverage and capacity in cellular system.

Q.2 Explain the following in brief –

(a) WDM

(b) Fiber optic cables

Q.3 Explain the AMPS and CDMA.

Q.4 Explain the transmitter and receiver for the followings –

(a) FSK

(b) QPSK

Q.5 Write the short note on –

(a) UWB

(b) Token Ring LAN

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7E1731

Roll No. _____ Total No. of Pages: 2

7E1731

B. Tech. VII - Sem. (Main / Back) Exam., March - 2022

Open Elective - I

7EC6 – 60.2 Micro and Smart System Technology

Time: 3 Hours **Maximum Marks: 120**

Min. Passing Marks: 42

Instructions to Candidates:

Attempt all ten questions from Part A, five questions out of seven questions from Part B and four questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 What are the hybrid smart materials?

Q.2 What is an intelligent system?

Q.3 List the functions of strain gauges.

Q.4 What is a silicon capacitive accelerometer?

Q.5 How the actuators are used in structure?

Q.6 Name the piezoelectric maternal used in smart structures.

Q.7 What are the geometrical processes?

Q.8 What is the silicon wafer processing?

Q.9 What is the wafer bonding and metallization?

Q.10 State the scaling issues in modelling.

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PART – B

(Analytical/Problem solving questions) **[5×8=40]**

Attempt any five questions

Q.1 Explain the functions of various sensing systems and actuating systems in smart structures.

Q.2 Discuss in detail the functions and response of instrumental structures.

Q.3 What are the different types of strain gauges in smart structures? Explain in brief.

Q.4 Explain the (i) passive sensory smart structure (ii) active sensing and reactive smart structure.

Q.5 What are the different actuator materials? Explain reactive actuator based smart structures.

Q.6 What is an optimized control algorithm? How does it help to perform the required functions after sensing changes?

Q.7 Explain the role of pressure transducer in smart structure.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[4×15=60]**

Attempt any four questions

Q.1 Explain –

(a) Thin film processing

(b) Smart material processing

Q.2 Explain the piezoelectric and piezoresistive modelling.

Q.3 Explain the following –

(a) Thermal cycler BEL pressure sensor

(b) Active vibration control of a beam

Q.4 Explain the LTCC multi-chip-module technology in detail.

Q.5 Explain –

(a) Micro gas turbine

(b) Silicon micro mirror arrays

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7E7081

Roll No. _____ Total No. of Pages: 2

7E7081

B. Tech. VII - Sem. (Back) Exam., January - 2022
Electronics & Communication Engineering
7EC1A Antenna & Wave Propagation

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

Q.1 What is meant by radiation pattern? Draw the radiation pattern of - [16]

(a) Directional antenna

(b) Isotropic antenna

OR

Q.1 Define the following parameters with respect to the antenna - [16]

(a) Radiation resistance

(b) Beam area

(c) Radiation intensity

(d) Directivity

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UNIT - II

Q.2 Four sources have an equal magnitude and are spaced $\lambda/2$ apart. Maximum field is to be in line with sources. Plot the field pattern of the array. [16]

OR

Q.2 A uniform linear array consists of 16 isotropic sources with a spacing of $\lambda/4$ and phase difference f = -90°. Calculate HPBW and effective aperture. [16]

UNIT - III

Q.3 Explain the special features of parabolic reflector antenna and discuss on different types of feed used with a neat diagram. [16]

OR

Q.3 Explain the structure and operation of slot antenna. Also derive the expression of its input impedance. [16]

UNIT - IV

Q.4 Write short notes on - [16]

(a) Surface wave tilting

(b) Space wave propagation

(c) Tropospheric propagation

(d) Duct propagation

OR

Q.4 Obtain an expression for space wave field component taking into an account a direct wave field component and a reflected wave from the earth surface. [16]

UNIT - V

Q.5 Calculate the critical frequency for a medium at which the wave reflects, if the maximum electron density is 1.24×10^6 electrons/cm^3. [16]

OR

Q.5 Explain the electrical properties of Ionosphere and discuss the effects of Earth's magnetic field on ionosphere radio wave propagation. [16]

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7E7072

Roll No. _____ Total No. of Pages: 4

7E7072

B. Tech. VII - Sem. (Back) Exam., March - 2022
Applied Electronics & Instrumentation Engineering
7AI2 Digital Signal Processing
AI, EC, EIC

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Draw block diagram of discrete time processing of continuous time signals and write mathematical expression in terms of time-domain and frequency-domain for output of each stage. [8]

(b) Determine the Nyquist rate and Nyquist interval for the signal - [8]

$$x(t) = \frac{1}{2\pi} \cos(4000\pi t) \cos(1000\pi t)$$

OR

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Q.1 (a) Let x(t) be a signal with Nyquist rate ω_0.

Also let $f(t) = x(t)\ \delta_T(t-1)$

Where $\delta_T(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT)$

and $T \propto \frac{2\pi}{\omega_0}$

Specific the constraints on the magnitude and phase of the frequency response of a filter that gives x(t) as its output when y(t) is the output. [10]

(b) What are interpolation techniques for the reconstruction of a continuous time signal from its samples? [6]

UNIT- II

Q.2 (a) Define all-pass system. Write -

(i) Generalized expression of an all-pass system. [4]

(ii) Discuss stability and causality condition for a discrete system having pole on the finite z-plane. [4]

(b) Define minimum phase system. A system is defined by –

$$H(z) = \frac{1+3z^{-1}}{1+\frac{1}{2}z^{-1}}$$

Express H(z) in terms of minimum and all-pass system. [4+4=8]

OR

Q.2 (a) Discuss the following by giving suitable mathematical expression. [2+3+3=8]

(i) Group delay

(ii) Linear phase system

(iii) Maximum phase system

(b) Find the difference equation of the system function of linear time invariant system.

$$H(z) = \frac{(1+z^{-1})^2}{\left(1-\frac{1}{2}z^{-1}\right)\left(1+\frac{3}{4}z^{-1}\right)}$$ [8]

UNIT- III

Q.3 Obtain the cascade and parallel form structure for - [16]

$$H(z) = \frac{(1-z^{-1})^3}{\left(1-\frac{1}{2}z^{-1}\right)\left(1-\frac{1}{8}z^{-1}\right)}$$

OR

Q.3 Consider the causal LTI system with the system function - [16]

$$H(z) = \frac{2-\frac{8}{3}z^{-1}-2z^{-2}}{\left(1-\frac{1}{3}z^{-1}\right)\left(1+\frac{2}{3}z^{-1}\right)}$$

Draw the structure for this system as –

(i) Direct form - I

(ii) Direct form - II

(iii) Parallel form first order direct form – II

(iv) Transposed parallel form first order direct form - II

UNIT- IV

Q.4 Design a Butterworth band elimination filter with the following specification - [16]

Passband ripple = 2 dB

Stop band ripple = 10 dB

Passband frequencies = 0.07π rad/sec and 0.8π rad/sec

Stop band frequencies = 0.02π rad/sec and 0.3π rad/sec

OR

Q.4 (a) Discuss frequency transformation for an analog filter into modified form of another analog filter by taking a suitable example and using mathematical expression. [8]

(b) An analog filter transfer function is defined as – [8]

$$H(s) = \frac{s+0.1}{(s+0.1)^2+16}$$

Obtain the system function of the digital filter using bilinear transformation which is resonant at $\omega_r = \frac{\pi}{2}$

UNIT- V

Q.5 (a) Explain the Coding-Decoding system of speech signal. [8]

(b) Given x(n) = {0, 1, 2, 3, 4, 5, 6, 7}, determine DFT using DIT- FFT algorithm. [8]

OR

Q.5 (a) Derive an expression representing circular frequency shifting property of DFT. [8]

(b) Find DFT of the sequence – [8]

$$x(n) = \begin{cases} 1; & 2 \leq n \leq 6 \\ 0; & n = 0, 1, 7, 8, 9 \end{cases}$$

Given N = 10

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7E7078

Roll No. _____ Total No. of Pages: 3

7E7078

B. Tech. VII - Sem. (Main / Back) Exam., March - 2022
Electronic Instrumentation & Control Engineering
7EI3A Digital Image Processing
EC, EIC

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Define image processing. Explain the representation of digital image using suitable diagram. [8]

(b) Explain spatial and gray level resolution. Briefly explain image sensing. [8]

OR

Q.1 (a) Explain the image sampling and quantization using suitable diagram. [8]

(b) Explain zooming and shrinking of digital images. Define spatial operation. [8]

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UNIT- II

Q.2 Explain the following – [8+8=16]

(a) Histogram equalization

(b) Intensity transformation functions

OR

Q.2 (a) What is the need of filtering of image in digital image processing? Explain the need of spatial filtering for image smoothing. [8]

(b) Explain the term image sharpening. Using first order derivatives, calculate image sharpness. [8]

UNIT- III

Q.3 (a) Define the term noise model. Explain the frequency properties of noise. [8]

(b) Define image restoration in brief. Explain the working principle of Wiener filtering. [8]

OR

Q.3 Explain the following – [8+8=16]

(a) Different noise probability density functions

(b) Role of adaptive filters

UNIT- IV

Q.4 (a) What is morphological image processing? Using suitable example explain Erosion. [8]

(b) Explain smoothing and thickening for morphological image processing. [8]

OR

Q.4 Explain the following –

(a) Explain opening and closing for morphological image processing. [8]

(b) Compare Erosion and Dilation. [8]

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UNIT- V

Q.5 (a) What is the need of image compression? Explain the basic principle of image compression using suitable diagram. [8]

(b) Compare loss-less and lossy compression technique for digital image processing. [8]

OR

Q.5 (a) Explain the need of image segmentation. Explain the working principle of edge based segmentation. [8]

(b) Explain the term Thresholding. Explain the watershed transform. [8]

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7E7083

Roll No. _____ Total No. of Pages: 2

7E7083

B. Tech. VII - Sem. (Back) Exam., January - 2022
Electronics & Communication Engineering
7EC4A Wireless Communication

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

Q.1 Explain the direct sequence and frequency hopping spread spectrum and derive the processing gain for both. [16]

OR

Q.1 Explain transmitter and receiver of DSSS with a suitable diagram. [16]

UNIT - II

Q.2 Define line of sight propagation and effect of Earth's curvature, also explain the Fresnel zone clearance the bending of radio beam. [16]

OR

Q.2 Make a block diagram of a microwave link and explain its operation. Also discuss the tropospheric scatter link. [16]

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UNIT - III

Q.3 What do you mean by multiple access in wireless communication? Discuss the three major access techniques used to share the available bandwidth in wireless communication network. [16]

OR

Q.3 Define briefly the operation a Time Division Multiple Access (TDMA) schemes. Also compare CDMA, TDMA and FDMA. [16]

UNIT - IV

Q.4 Describe GSM cellular architecture and its various features .What are the various standards used in GSM cellular telephony? [16]

OR

Q.4 A hexagonal cell within a four-cell has a radius of 1.387 km. A total of 60 channels are used within the entire system. If the load per user is 0.039 Erlangs and a λ =1 call/hr. Compute the following for an Erlang C system that has a 5% probability of a delayed call - [16]

(i) How many user per square km will this system support?

(ii) What is the probability that a delayed call will have to wait for more than 10 seconds?

(iii) What is the probability that a call will be delayed for more than 10 seconds?

UNIT - V

Q.5 Explain all parts of satellite earth station with block diagram and example. [16]

OR

Q.5 Explain routing, localization and handover in satellite communication. [16]

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7E7084

Roll No. _____ Total No. of Pages: 2

7E7084

B. Tech. VII - Sem. (Main / Back) Exam., January - 2022
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

Q.1 (a) Describe the enhancement mode and depletion mode MOS transistor with the help of their structure and working. [8]

(b) Determine the relationship between I_{ds} and V_{ds} for MOSFET and modify it for channel length modulation. [8]

OR

Q.1 (a) Discuss about the different techniques of CMOS fabrication? Explain the various steps involved in CMOS n-well fabrication. [8]

(b) Find the expression of threshold voltage and discuss, how it is modified under body bias? [8]

UNIT - II

Q.2 (a) Derive an expression of pull up/pull down ratio for complementary metal oxide semiconductor transistor. [5]

(b) Describe the significance of (β_n/β_p) ratio of CMOS inverter. [5]

(c) Describe the structure of CMOS transmission gate. [6]

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OR

Q.2 (a) Design the following CMOS logic - [8]

(i) $Y = \overline{A + BC + DE}$

(ii) $Y = (A + B + C)(D + E)$

(iii) $Y = AB + \overline{AB}$

(b) What do you meant by noise margin? Explain the procedure determine the noise margin. [8]

UNIT - III

Q. 3 (a) Draw the layout of given function and then optimize the same with the help of Euler's graph - [6]

$F = \overline{A(D + E) + BC}$

(b) What do you mean by latch up problem in MOS circuits? Draw the suitable diagram and explain it. [6]

(c) Draw the layout of 3-input NAND. [4]

OR

Q.3 (a) What do you mean by layout design rules? [4]

(b) Draw the layout of 3-input NOR and 3-input AND gate. [6]

(c) What is Euler path? Find the Euler path for $F = \overline{(D + E + A)(B + C)}$ and draw its stick diagram. [6]

UNIT – IV

Q.4 (a) Describe the basic architecture of zipper CMOS circuit. [8]

(b) Classify and explain all the types of ROM memories. [8]

OR

Q.4 (a) Compare the SRAM and DRAM cell in detail. [8]

(b) Explain the C^2 MOS logic in detail. [8]

UNIT – V

Q.5 (a) Write VHDL code for - [8]

(i) J-K flip flop

(ii) T flip flop

(b) Explain the ECAD tools for first and back end design of VLSI circuits. [8]

OR

Q.5 (a) Write a VHDL code for 4:1 multiplier in behavioral style of modeling. [8]

(b) Write a VHDL code for a 3-bit left to right shift register. [8]

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7E7086

Roll No. _____ Total No. of Pages: 2

7E7086

B. Tech. VII - Sem. (Main / Back) Exam., January - 2022
Electronics & Communication Engineering
7EC6.3A VHDL

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

Q.1 (a) Explain the place route and timing simulation. [8]

(b) What is VHDL? Describe, how variables, signal and constants are declared and used inVHDL. [8]

OR

Q.1 (a) What is PLD? Describe, how different types of PLD. [8]

(b) What is the advantage of VHDL digital design over the traditional methods? [5]

(c) Describe design flow of ASICs. [3]

UNIT - II

Q.2 (a) Explain data flow, structural, behavioral and RTL Style of combinational design. [8]

(b) Explain event-driven simulation and simulation approaches. [8]

OR

Q.2 (a) What is modeling? Explain behavioral and structural modeling in detail. [8]

(b) Explain elaboration signal driver simulator kernel process. [8]

UNIT - III

Q.3 (a) Write 4-bit comparator VHDL Code. [8]

(b) Write VHDL Code for implementing D flip-flop using a WAIT-UNTIL statement. [8]

OR

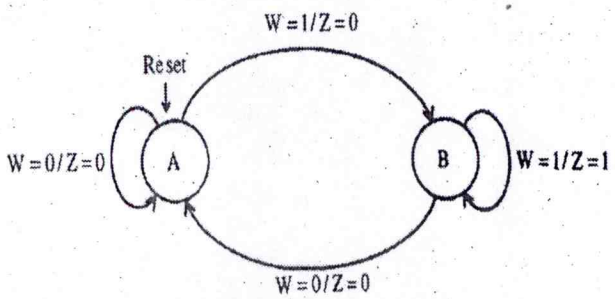
Q.3 (a) Write a VHDL Code for 1:16 line decoder. [8]

(b) Consider the function $Y = \bar{A}BC + \overline{ABC} + AB\bar{C}$ Implement the above function using 2:1 multiplayer and also write VHDL Code for it. [8]

UNIT - IV

Q. 4 (a) State the difference between Mealy and Moore type FSM. [8]

(b) Write a VHDL Code for given state diagram Mealy type FSM. [8]



OR

Q.4 (a) Write short note on Vending Machine with a suitable example. [8]

(b) Write a VHDL Code for Serial Adder and also explain one hot encoding. [8]

UNIT - V

Q. 5 (a) Explain SRAM in brief and what is clock skew and how it can be minimized? [8]

(b) Draw the schematic diagram of data path circuit for multiplier operation. [8]

OR

Q.5 (a) Describe CPU organization and also explain its design concept. [8]

(b) Write a VHDL Code for shorting operation and Multiplier. [8]
