7E7081

Roll No. _____ Total No of Pages: 3

7E7081

B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021

Electronics & Communication Engineering

7EC1A Antenna & Wave Propagation

Time: 2 Hours **Maximum Marks: 48**

Min. Passing Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Define and explain the following terms of antenna - [8]

(i) Beam – width

(ii) Directivity

(iii) Effective aperture

(iv) Antenna efficiency

(b) What are the roles of an antenna in wireless technology? Explain how the concept of displacement current was introduced by Maxwell to account for the production of magnetic field in free space. [8]

OR

Q.1 (a) With the help of Maxwell's equation, explain how radian and reception of EM wave takes place. Isotropic radiator is only a theoretical concept; it cannot be designed practically. Why? [8]

(b) An antenna has normalized radiation intensity U (θ, $\varnothing$) = 10 sinθ sin$\varnothing$; W/sr for $0 < \theta < \Pi$ and $0 < \varnothing < 2\Pi$ and zero elsewhere. Find the radiated power and directivity. [8]

UNIT- II

Q.2 What is phased array antenna? What is the main difference between BSA and EFA? Plot the normalized field pattern for BSA and EFA by considering an array of eight elements spaced at $\lambda/2$. [16]

OR

Q.2 Define the principle of pattern multiplication of an antenna array. A uniform linear array consists of 14 isotropic point sources with spacing of $\lambda/4$. Calculate- [16]

(a) Directivity

(b) Effective aperture, if the phase difference $\psi = -90°$

UNIT- III

Q.3 (a) Design a three-element Yagi – Uda antenna to operate at a frequency of 570 MHz. [6]

(b) What are the different categories of lens antennas? Explain the basic principle of operation of a dielectric lens antenna showing how it converts a spherical wave front into a plane wave front. Also derive the lens equation. [10]

OR

Q.3 (a) Calculate the design data of a rhombic antenna to operate at 50 MHz if the angle of elevation is 30°. [6]

(b) Design a rectangular micro – strip patch with dimensions W and L over a single substrate, whose center frequency is 10 GHz. The dielectric constant of the substrate is 10.2 and the height of the substrate is 0.127 cm. Determine the physical dimensions W and L (in cm) of the patch, taking into account field fringing. [10]

UNIT- IV

Q.4 (a) Explain the formation of ionosphere. What are the various layers of the ionosphere and their effects on wave propagation? With the help of a neat diagram show their height from the ground. [8]

(b) Explain with suitable diagram the "Multiple Hop Transmission". Also describe the effect of earth's magnetic field on ionosphere wave propagation. [8]

OR

Q.4 (a) What do you understand by duct propagation? Under what conditions are ducts formed? Discuss the frequency bands useful for duct propagation. What are its main limitations? [8]

(b) What is tropospheric scattering? What is the frequency range for it? What are the major conditions for its operation? [8]

UNIT- V

Q.5 (a) Define the critical frequency and critical angle. How is critical frequency and critical angle related with electron density? [4]

(b) What are the effects of ground on antennas? What are grounded and ungrounded antennas? [4]

(c) A communication system is to be established at a frequency of 60 MHz with a transmitter power of 2kW. The field strength of the directive antenna is 5 times that of a half – wave antenna, $h_t = 60mm$, $h_r = 6m$. Field strength of 100 $\mu V/m$ is required to give satisfactory reception. Find the range of the system. [8]

OR

Q.5 (a) What is meant by fading? Also define skip distance and give the reasons why it varies. [4]

(b) Find the critical frequency if the maximum electron density is 1.3×10^6 electron/cm^3. Also calculate the critical angle of propagation for D-layers if the transmitter and receiver are separated by 450 km. [4]

(c) A high frequency radio link has to be established between two points at a distance of 2500 km on earth's surface. Considering the ionospheric height to be 200 km and its critical frequency 5MHz, calculate the Maximum Usable Frequency (MUF) for the given path. [8]

7E1729

Roll No. _____ Total No. of Pages: 3

7E1729

B. Tech. VII - Sem. (Main) Exam., Feb.- March - 2021
PEC Electronics & Communication Engineering
7EC5 – 13 CMOS Design

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 82

Min. Marks: 29

Instructions to Candidates:

Attempt all ten questions from Part A, four questions out of seven questions from Part B and two questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Mention any two difference between CMOS and Bipolar technology.

Q.2 How transistor works as a switch?

Q.3 Draw the stick diagram for 2 input NAND gate.

Q.4 Draw the layout for $\overline{Y} = A + BC$ using CMOS.

Q.5 What are the layout issues for CMOS inverter?

Q.6 Briefly explain ECAD tools.

Q.7 Explain non ideal IV effects of MOSFET.

Q.8 Explain SRAM in brief.

Q.9 Explain NP (ZIPPER) logic in brief.

Q.10 Define Regularity.

PART – B

(Analytical/Problem solving questions) **[4×8=32]**

Attempt any four questions

Q.1 Write all the mask steps of P-well process.

Q.2 Explain Noise margin with respect to CMOS inverter.

Q.3 Explain two transistor dynamic RAM with neat circuit and stick diagram.

Q.4 Explain the goals and techniques of FPGA based system design.

Q.5 With the help of block diagram, explain the process of Logic Fabrication.

Q.6 Explain RC Delay Model Layout.

Q.7 Derive the expression of delay in terms of τ for CMOS inverter pair.

PART – C

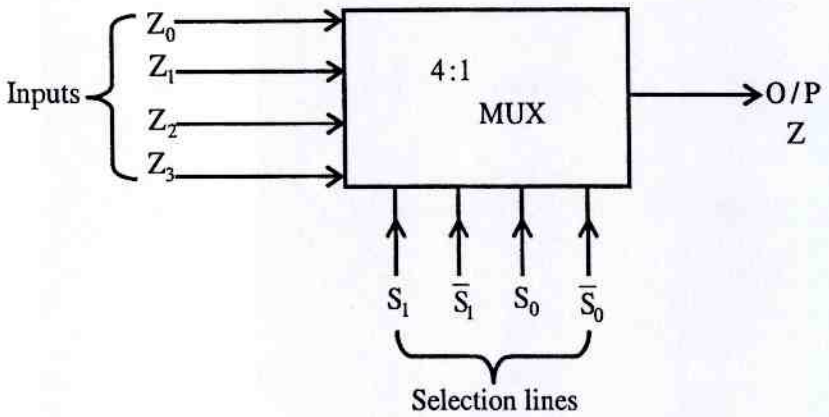
(Descriptive/Analytical/Problem Solving/Design Questions) **[2×15=30]**

Attempt any two questions

Q.1 Discuss the different design rules in transistors (NMOS, PMOS and CMOS).

Q.2 Draw the block diagram of Generic structure of an FPGA fabric and explain it.

Q.3 Construct a stick diagram for a multiplexer using COMS -



Q.4 Explain the following logics –

(a) Clocked CMOS logic

(b) DOMINO logic

(c) NORA logic

Q.5 Explain the CMOS inverter DC characteristics. Highlighting the regions of operation.

7E1727

Roll No. _____ Total No. of Pages: 2

7E1727

B. Tech. VII - Sem. (Main) Exam., Feb.- March - 2021
PEC Electronics & Communication Engineering
7EC5 – 11 VLSI Design

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 82

Min. Marks: 29

Instructions to Candidates:

Attempt all ten questions from Part A, four questions out of seven questions from Part B and two questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 Write down the equations for Ids of an n-channel enhancement MOSFET operating in Non-saturated region and saturated region.

Q.2 Draw the circuit diagram for CMOS two-input NAND gates.

Q.3 Draw the basic circuit of NMOS and CMOS inverter.

Q.4 What are the advantages and disadvantages of dynamic logic?

Q.5 What parameters to be consider while identifying the FPGA?

Q.6 What is NORA CMOS?

Q.7 What is meant by channel length modulation in NMOS transistors?

Q.8 Differentiate between SRAM and DRAM?

Q.9 Draw a 1 – Transistor dynamic RAM cell.

Q.10 Mention different clocking mechanisms.

PART – B

(Analytical/Problem solving questions) **[4×8=32]**

Attempt any four questions

Q.1 What is threshold voltage of a MOS device and explain its significance.

Q.2 Prove that the pull-up to pull-down for NMOS inverter is 4:1 when it is driven by another inverter.

Q.3 What is "Euler path"? What is use of it? Explain with a suitable example.

Q.4 Draw the CMOS logic circuit for the Boolean expression Z=[A(B+C) +DE] and explain.

Q.5 What is a stick diagram and explain about different symbols used for components in stick diagram?

Q.6 Derive the propagation delay for NMOS inverter?

Q.7 Explain the Domino logic with neat diagram.

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[2×15=30]**

Attempt any two questions

Q.1 Explain the dynamic behavior of MOSFET transistor with neat diagram.

Q.2 Write the layout design rules and draw diagram for four input NAND and NOR gate.

Q.3 Explain the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.

Q.4 Explain about building block architecture of FPGA.

Q.5 What do you mean by VHDL? Write a VIDL code for-

(a) Full Adder

(b) D Flip-flop

7E1723

Roll No. _____ Total No. of Pages: 2

7E1723

B. Tech. VII - Sem. (Main) Exam., Feb.- March - 2021
OE -I Open Elective-I Computer Science & Engineering
7CS6 – 60.2 Cyber Security

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 82

Min. Marks: 29

Instructions to Candidates:

Attempt all ten questions from Part A, four questions out of seven questions from Part B and two questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 What do you understand by a global perspective on cybercrimes?

Q.2 Define Copyright Act.

Q.3 What do you understand by password cracking?

Q.4 What is the need of WWW policies?

Q.5 Define Cloud Computing.

Q.6 What do you know the buffer overflow?

Q.7 Differentiate the term virus and worms.

Q.8 Explain authentication service security.

Q.9 What do you mean by disposal of data?

Q.10 What is information assurance?

PART – B

(Analytical/Problem solving questions) **[4×8=32]**

Attempt any four questions

Q.1 What is cybercrime? Explain classifications of cybercrimes.

Q.2 What is the security architecture of information systems? Explain the secure system design of information system.

Q.3 Explain the following terms –

(a) Cybercrime and Indian ITA 2000

(b) SQL injection

Q.4 What is security association? Discuss the parameters used to describe security association.

Q.5 What do you know about threats? Explain web threats for organizations in detail.

Q.6 Explain the Botnets the fuel for cybercrime.

Q.7 What you know about different type of attacks?

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[2×15=30]**

Attempt any two questions

Q.1 What is the need of Risk Management? What are the processes in value to managing the risk during the development of secure information?

Q.2 What is the Intellectual Property Right? Explain the various types of Intellectual Property Rights and IPR issues.

Q.3 What is phishing? Explain Trojan Horse and Backdoors Steganography.

Q.4 What is Social Engineering? Explain Attack Vector.

Q.5 What is mobility? Explain trends in mobility.

7E7072

Roll No. _____ Total No of Pages: 2

7E7072

B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Applied Electronics & Instrumentation Engineering
7AI2 Digital Signal Processing
AI, EC, EIC

Time: 2 Hours **Maximum Marks: 48**
Min. Passing Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain Sampling theorem. Give necessary condition of sampling. [8]

(b) Discuss the method of continuous time processing of discrete time signals. [8]

OR

Q.1 What are sampling rate alteration devices? How can we increase or decrease the sampling rate using discrete time processing? [16]

UNIT- II

Q.2 (a) Obtain a linear convolution of following two discrete time signals - [8]

$$x(n) = \sum_{k=0}^{2} \delta(n-k)$$

(b) State and explain properties of linear convolution. [8]

OR

Q.2 Find out the particular solution for the following differential equation - [8×2=16]

(a) $y(n) + 3y(n-1) = x(n)$

(b) $y(n) + 3y(n-1) - 4y(n-2) + x(n)$

UNIT- III

Q.3 (a) Draw and explain block diagram representation for discrete time LTI system. [8]

(b) Draw the block diagram representation in direct form, cascade form for following LTI system expressed by transfer function - [8]

$$H(z) = \frac{1}{\left(1+\frac{1}{3}z^{-1}\right)\left(1-\frac{1}{6}z^{-1}\right)}$$

OR

Q.3 (a) What are IIR and FIR filters? Draw basic structures for them and explain. [8]

(b) List out the advantages and disadvantages of digital filters over analog filters. [8]

UNIT- IV

Q.4 Determine H(z) using impulse invariance method at 5Hz sampling frequency from Ha(s) as given below - [16]

$$\left[Ha(s)= \frac{2}{(s+1)(s+2)}\right]$$

OR

Q.4 (a) Explain design technique of FIR filters using - [12]

(i) Rectangular window

(ii) Hamming window

(iii) Kaiser window

(b) Using Chebyshev filter approximation explain type I filter design. [4]

UNIT- V

Q.5 (a) What is Discrete Fourier Transform? List out the properties of DFT. [6]

(b) Compute N-point DFT of the following exponential sequence - [10]

$$x(n) = a^n u(n) \qquad \text{for} \qquad 0 \le n \le N-1$$

OR

Q.5 Determine the 8 point DFT of the following sequence - [16]

$$x(n)= \left[\frac{1}{2}, \frac{1}{2}, \frac{1}{2}, \frac{1}{2}, 0, 0, 0, 0\right]$$

7E1731

Roll No. _____ Total No. of Pages: 3

7E1731

B. Tech. VII - Sem. (Main) Exam., Feb.- March - 2021

OE -I Open Elective-I Electronics & Communication Engineering

7EC6 – 60.2 Micro & Smart System Technology

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 82

Min. Marks: 29

Instructions to Candidates:

Attempt all ten questions from Part A, four questions out of seven questions from Part B and two questions out of five from Part C.

Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used /calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

PART – A

(Answer should be given up to 25 words only) **[10×2=20]**

All questions are compulsory

Q.1 What is Smart material system? [2]

Q.2 What is Microsystem? [2]

Q.3 Write down the application areas of microsystems. [2]

Q.4 Write down the advantages of electro-thermal actuator. [2]

Q.5 Draw the block diagram of conductometric gas sensor. [2]

Q.6 What is lithography? Write down the types of lithography. [2]

Q.7 Write down the difference between wet and dry etching. [2]

Q.8 What is Piezoresistive modeling? [2]

Q.9 What is thermal loading? [2]

Q.10 What is multichip module technology? [2]

PART – B

(Analytical/Problem solving questions) **[4×8=32]**

Attempt any four questions

Q.1 Explain the working of Micro-machined transducers, with the help of neat and clean diagram. [8]

Q.2 Write down the name of components of a smart system. Explain all the component in brief. [8]

Q.3 What is silicon capacitive accelerometer? Write down the advantage of this sensor. Explain with circuit diagram. [8]

Q.4 Explain with the help of neat and clean diagram of wafer – bonding and metallization process in Silicon wafer processing. [8]

Q.5 Explain the block diagram of coupled electro-mechanics and capillary electrophoresis. [8]

Q.6 How can measure the Elastic deformation and analysis the stress of beams and plates? [8]

Q.7 Draw the flow diagram of Thermal Cycler for DNA amplification. Explain all the steps in brief. [8]

PART – C

(Descriptive/Analytical/Problem Solving/Design Questions) **[2×15=30]**

Attempt any two questions

Q.1 How can integrate of microelectronics and micro-devices at wafer and chip levels. Also explain the packaging process in Microelectronic. [15]

Q.2 What are the component of electrostatics used in modelling? Explain it and also explain the scaling issues in Modeling. [15]

Q.3 Explain the following terms - [15]

(a) Thin-film deposition

(b) Thick – film processing

(c) Smart material processing

(d) Emerging trends

(e) Magnetic micro relay

Q.4 What are the difference between Sensors and Actuators? Explain the working principle, circuit diagram and advantages of surface acoustic wave based wireless strain sensor. [15]

Q.5 Draw the structure of Smart material system. Also explain the components, applications and commercial products of smart materials systems. [15]

7E7078

Roll No. _____ Total No of Pages: 2

7E7078

B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Electronics Instrumentation & Control Engineering
7EI3A Digital Image Processing
EC, EIC

Time: 2 Hours **[To be converted as per scheme]**

Max. Marks: 48

Min. Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit.** All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Discuss down sampling (or subsampling) and up sampling of an image with suitable example. [8]

(b) Discuss working of image acquisition system by using CCD sensors. [8]

OR

Q.1 (a) What are the basic components of a digital image processing system? Write down the three examples of a field that use digital image processing. [8]

(b) Explain the basic concepts in sampling and quantization digital image processing. [8]

UNIT- II

Q.2 Describe the various types of frequency domain filters. [16]

OR

Q.2 (a) Discuss image sharpening by using second order derivative with an example. [8]

(b) Explain why the discrete histogram equalization technique does not, in general yield a flat histogram. [8]

UNIT- III

Q.3 (a) Discuss working of order static filter and their suitable application in image processing. [8]

(b) Explain the adaptive median filter and also write its application. [8]

OR

Q.3 (a) Explain the noise estimation parameter. [8]

(b) Explain the concepts of Inverse and Wiener filtering. [8]

UNIT- IV

Q.4 (a) Discuss image opening morphological operation by writing its mathematical representation. [8]

(b) Discuss image closing morphological operation by using its mathematical representation. [8]

OR

Q.4 (a) Explain Erosion and Dilation. [8]

(b) Explain-

(i) Thickening [4]

(ii) Pruning [4]

UNIT- V

Q.5 (a) Discuss watershed transform along with its suitable application. [8]

(b) Discuss any one lossless compression technique and state advantages of lossless compression. [8]

OR

Q.5 (a) Discuss image segmentation based on global thresholding. [8]

(b) Explain the fundamentals of edge-based segmentation. [8]

7E7083

Roll No. _____ Total No of Pages: 3

7E7083

B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Electronics & Communication Engineering
7EC4A Wireless Communication

Time: 2 Hours **Maximum Marks: 48**
Min. Passing Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the DSSS with binary phase shift keying and compare its performance with FHSS. [8]

(b) Write the properties of PN sequence. If the chip rate of a DSSS transmitter is 20Mbps, the message bit rate is 10 kbps. Find out the processing gain achieved, if bpsk is used. [2+6=8]

OR

Q.1 (a) Explain FHSS with basic block diagram and find the expression for processing gain (G_p) in fast and slow systems. [8]

(b) Explain the properties of spreading codes. How are they generated? Briefly explain. [8]

UNIT- II

Q.2 (a) Explain the transmitter and receiver block diagram of Microwave link. [8]

(b) Explain the concept of diffraction loss as a function of path difference around an obstruction by Fresnel zones. [8]

OR

Q.2 (a) Explain small scale fading and write the time dispersion parameters. [8]

(b) Assume a receiver is 20 km from a 100W transmitter. The carrier frequency is 1000 MHz free space propagation is assumed, $G_t = 1$ and $G_r = 3$. Find the power at the receiver. [8]

UNIT- III

Q.3 (a) Explain the TDMA principle of operation with TDMA/TDD example. Write its advantages and disadvantages and efficiency. Also, compare FDMA with TDMA. [8+2=10]

(b) If a normal GSM time slot consists of 6 trailing bits, 8.25 guard bits, 26 training bits and 2 traffic bursts of 61 bits of data, find the frame efficiency. [6]

OR

Q.3 (a) Briefly explain the Near-Far problem in both uplink and downlink of CDMA. [6]

(b) Explain the CDMA principle of operation with its advantages and disadvantages. Which type of Handoffs occur in CDMA mobile systems? [10]

UNIT- IV

Q.4 (a) Explain the process of speech coding in GSM. [6]

(b) Define Handoff and Handovers in GSM. [6]

(c) Compare WiFi and WiMax Technology. [4]

OR

Q.4 (a) Explain RFID Technology [6]

(b) Explain briefly -

(i) Bluetooth [5]

(ii) Broadband wireless 1002.16 [5]

UNIT- V

Q.5 Write short notes on the following -

(a) Low Noise Amplifier [4]

(b) Up converter [4]

(c) Down converter [4]

(d) Monitoring and control [4]

OR

Q.5 (a) Explain the process of link design of a satellite system and derive an expression for the received power. [8]

(b) Define the following -

(i) Coverage angle [2]

(ii) Slant range [2]

(iii) Orbital period [2]

(iv) Orbital velocity [2]

7E7084

Roll No. _____ Total No of Pages: 3

7E7084

B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 2 Hours **Maximum Marks: 48**
Min. Passing Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination.

(Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Draw and write the working of enhancement mode PMOS with the help of input-output and transfer characteristics. [8]

(b) Write the names and compare the three technologies used for the fabrication of CMOS transistor. [8]

OR

Q.1 (a) What are the different factors affecting the threshold voltage of MOSFET? Derive the formula used. Also, derive the body effect coefficient. [8]

(b) Draw MOS transistor circuit model and explain the origination of each parameter. [8]

UNIT- II

Q.2 (a) Draw voltage transfer characteristics (VTC) of CMOS inverter and derive the expression for Bn/Bp ratio. [8]

(b) Write the names of three types of power dissipation in CMOS logic circuits and derive the expression for total power dissipation. [8]

OR

Q.2 (a) Design the following logic circuits using CMOS logic gate – [8]

(i) 3 – input NAND gate

(ii) S–R Flip-flop

(b) Implement the Boolean expression F' = a. (b + b'c') using CMOS logic and also determine the size of each transistor using equivalent inverter transistor sizes. [8]

UNIT- III

Q.3 (a) Implement 2×1 multiplexer using transmission gate and draw its layout. [8]

(b) Draw Euler path and layout diagram for 3-input NOR gate and mark all the size/spacing using λ -rules. [8]

OR

Q.3 (a) What is latch-up problem in CMOS? Draw and explain its physical origin, model and V–I characteristics. [8]

(b) Write the names and explain the techniques used to prevent latch-up problem. [8]

UNIT- IV

Q.4 (a) Compare NORA and NP(ZIPPER) CMOS logic structures. [8]

(b) Explain various circuit techniques used in domino CMOS circuits for solving charge sharing problem. [8]

OR

Q.4 (a) Draw a circuit diagram of a DRAM cell and explain the following operations– [8]

(i) Synchronous read mode

(ii) Asynchronous read mode

(iii) Leakage currents and refresh operation

(b) Draw SRAM cell and explain its write and read operation with appropriate timing diagram. [8]

UNIT- V

Q.5 (a) Draw VHDL/PLD based ASIC design flow block diagram. Explain each step involved. [8]

(b) Write VHDL code for positive edge triggered S-R flip-flop. [8]

OR

Q.5 (a) Write VHDL code for half adder in structural style. [8]

(b) Write VHDL model for left to right shift register using enable input. [8]

7E7085

Roll No. _____ Total No of Pages: 3

7E7085

B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Electronics & Communication Engineering
7EC6.1A Advanced Microprocessors
Common for EC, EIC

Time: 2 Hours **Maximum Marks: 48**
Min. Passing Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit.** All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the architecture of 8086 microprocessor and its minimum and maximum mode operations in detail. [8]

(b) Explain different hardware and software interrupts in 8086 MP. What is significance of IVT in interrupt handling? [8]

OR

Q.1 (a) Explain the addressing modes of 8086 microprocessor with examples. [8]

(b) What are the conditions that will cause BIU to suspend fetching instructions? Under what conditions will the content of the queue hold "Wrong Op-codes"? [8]

UNIT- II

Q.2 (a) Write an 8086 based assembly language program to reverse the user entered string using macros. [8]

(b) Explain the following instructions of 8086 MP with examples- [8]

(i) AAM

(ii) AAD

(iii) SCASB

(iv) CMPSB

OR

Q.2 (a) Write an 8086 assembly language program to generate a square wave of 1 kHz at one of the bit of the output port. The 8086 MP is running at 5 MHz. Show the delay calculations. [8]

(b) Explain the following instructions of 8086 MP with examples- [8]

(i) DAA

(ii) INT

(iii) JS

(iv) DAS

UNIT- III

Q.3 (a) Explain the procedure for serial data communication in 8086 MP. Mention the pins and instructions of 8086 MP which participate in serial data communication. [8]

(b) Interface an 8-bit DAC with 8086 MP. Write an assembly language program to generate a sine wave. Give necessary comments. [8]

OR

Q.3 (a) List the procedure to setup TRAP in 8086 microprocessor. What is the significance and use of TRAP in 8086 MP? [8]

(b) Explain the IEEE 488 parallel data communication in 8086 MP.Mention the instructions in 8086 MP which participate in IEEE 488 communication. [8]

UNIT- IV

Q.4 Design an 8086 based system with the following specifications- [16]

(a) 8086 processor working at 8 MHz

(b) 64KB EPROM using 27256 chip

(c) 64 KB RAM using 622256 chip

(d) Two 16-bit input and output ports in handshake mode

Draw the necessary interfacing diagram, memory map and I/O map. Use absolute decoding technique. Explain the design.

OR

Q.4 Draw the interfacing diagram for the 8086 based system configuration in maximum mode with the following specifications- [16]

(a) 8086 working at 5 MHz

(b) 16 KB EPROM device

(c) 32 KB SRAM device to include IVT

(d) IC 8279 is interfaced

Use full decoding technique and draw the memory map for the above interface. Mention the addresses of different components involved.

UNIT- V

Q.5 (a) What is Pipelining? Explain the term with reference to 8086 MP. [8]

(b) Explain the Real and Virtual mode in 80286 MP. Explain the mapping of virtual memory and physical memory and mention the phenomenon of page table in microprocessors. [8]

OR

Q.5 (a) What are Pipeline Conflicts? Explain the hardware technique to handle the branch instructions. [8]

(b) What is Stack? Give the organization of register stack with all the necessary elements in 8086 and 80286 microprocessors. [8]

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B. Tech. VII - Sem. (Back) Exam., Feb.-March - 2021
Electronics & Communication Engineering
7EC6.3A VHDL

Time: 2 Hours **Maximum Marks: 48**
Min. Passing Marks: 15

Instructions to Candidates:

*Attempt **three questions,** selecting **one question each** from any three **unit**. All Questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/ calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No.205)

1. NIL 2. NIL

UNIT- I

Q.1 Explain the following terms in VHDL-

(a) Functional Simulation [4]

(b) Timing Simulation [4]

(c) Design Flow [4]

(d) Design Methodology [4]

OR

Q.1 Write VHDL code for -

(a) Full Adder [4]

(b) 2 × 1 MUX [4]

(c) 3 – input NOR gate [4]

(d) SR – Latch [4]

UNIT- II

Q.2 How the following is defined/written in VHDL -

(a) Event –driven Simulation [4]

(b) Data Types [4]

(c) Signals Verses Variables [4]

(d) Packages [4]

Explain with an example.

OR

Q.2 (a) Write VHDL code for a 4 – bit down counter using sequential statements. [8]

(b) Define elaboration signal driver using an example. [8]

UNIT- III

Q.3 (a) Write VHDL code for a 4 – bit shift register. [8]

(b) Write VHDL code for a code converter (Consider any one example). [8]

OR

Q.3 (a) Write VHDL code for JK flip-flop in two styles. [8]

(b) Write a VHDL code for 7 – segment to BCD code converter using select signal assignment. [8]

UNIT- IV

Q.4 (a) Write a VHDL code for a Moore m/c and explain the general procedure for such a m/c. [8]

(b) Identify shift register as Moore or Mealy m/c and write its VHDL code accordingly. [8]

OR

Q.4 Write a VHDL code for a Vending Machine that delivers tea at a cost of ₹ 5 and accepts coins of ₹ 1, ₹ 2 and ₹ 5. [16]

UNIT- V

Q.5 (a) How memory organization is defined in VHDL? Write a VHDL code to organize 10k (SRAM) memory. [8]

(b) Explain the clock synchronization in VHDL. [8]

OR

Q.5 (a) Design a 4-bit divider and draw its flow diagram. Then write the VHDL code for it. [10]

(b) Explain shifting & sorting operation in VHDL. [6]
