7E4051

Roll No. _____ Total No of Pages: 4

7E4051

B. Tech. VII Sem. (Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC6.3 (O) Operating System

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Define Operating System. Explain how operating system acts as a resource manager? Differentiate between Multiprogramming and Multi-processing? [8]

(b) What is the difference between User level threads & Kernel level threads? Under what circumstance is one type better than the other? [8]

OR

Q.1 (a) What are the different services provided by the operating system? Explain all of them in detail. [8]

(b) What are the six major activities of an operating system with regards to file management? [8]

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UNIT- II

Q.2 (a) What is a process? What is the difference between a program and a process? Explain PCB using suitable example. [8]

(b) Define Scheduling criteria. Explain Quenching diagram for the CPU scheduling in detail. [8]

OR

Q.2 (a) In-connection with inter process communication explain the following: [8]

(i) Race condition

(ii) Critical condition

(iii) Sleep & Wake up

(iv) System call

(b) Consider the following set of processes with arrival time and CPU burst time given in ms. [8]

Process	Arrival time	Burst time
P_1	0	8
P_2	1	4
P_3	2	9
P_4	3	5

What is the average waiting time for these processes with pre-emptive SJF scheduling? [8]

UNIT- III

Q.3 Explain the Page – replacement algorithm. [16]

OR

Q.3 (a) What is the difference between Pager and Swapper? [4]

(b) What is demand paging? [4]

(c) What is thrashing? [4]

(d) Write short note on TLB. [4]

UNIT- IV

Q.4 (a) Explain various disk scheduling algorithm in brief. [8]

(b) What are the various access methods for file system? [8]

OR

Q.4 Explain the following:

(a) Tree structured directory [4]

(b) Spooling [4]

(c) File system mounting [4]

(d) Memory mapped files [4]

UNIT- V

Q.5 (a) What is deadlock? What are the necessary conditions for deadlock to occur? [8]

(b) Explain the following : [8]

(i) Resource allocation graph

(ii) Recovery from deadlock

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OR

Q.5 (a) Explain the difference between internal & external fragmentation. [8]

(b) Explain the following : [8]

(i) Logical & Physical address space

(ii) Dynamic linking

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7E4047

Roll No. _____ Total No of Pages: 3

7E4047

B. Tech. VII Sem. (Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC4 (O) IC Technology

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Discuss various steps for wafer preparation from the Si ingot obtained after CZ or FZ Method. [6]

(b) Explain the different kinds of crystal defects. [5]

(c) In a CZ growth, if the density of solid silicon is 1.4×10^{-3} gm/cm^3, thermal conductivity of solid is 7.6×10^{-4} mho and thermal gradient at the interface is 0.4, then find out the maximum pull rate. Assume the latent heat of fusion is 1.5J. [5]

OR

Q.1 (a) What is Czochralski Growth? Differentiate between pull rate and growth rate. Can pull rate become negative? If yes, explain why? [6]

(b) What do you understand by MGS and EGS? How is EGS obtained from MGS? [5]

(c) Find the concentration of boron in crystal at a fraction solidified of 0.5, if C_s at X=0.04 is 2×10^{18} and segregation coefficient is 0.8. [5]

UNIT- II

Q.2 (a) Write five specifications for electronic grade silicon. [4]

(b) What are "charged defects"? What is their origin and how these affect the electronic performances? [4]

(c) What do you mean by "solubility limit"? If we dissolve more than this limit, how it increases the defects? [4]

(d) Compare Czochralski and Float zone refine method from the following points of view : [4]

(i) Yield

(ii) Purity

(iii) Economic

OR

Q.2 (a) Develop Fick's law of diffusion. Write their solutions for constant surface concentration and constant total dopant for constant diffusivities. Clearly state the boundary conditions for both cases. [8]

(b) Explain the deal grove model of oxidation and discuss the effects of presence of water, sodium and halogens on oxidation. [8]

UNIT- III

Q.3 Explain the following in detail -

(a) Chemical equilibrium and law of mass action. [8]

(b) Low pressure CVD of dielectric and semiconductor. [8]

OR

Q.3 Discuss Vapour phase epitaxy and Molecular beam epitaxy. [16]

UNIT- IV

Q.4 Explain photo lithography and proximity printers with suitable diagram. [16]

OR

Q.4 Write notes on types of etching. [16]

UNIT- V

Q.5 Write short note on the following -

(a) LOCOS Methods [8]

(b) Trench Isolation [8]

OR

Q.5 Write short note on the following -

(a) Metallization [8]

(b) Planarization [8]

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7E4048

Roll No. _____ Total No of Pages: 3

7E4048

B. Tech. VII Sem. (Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC5 (O) VLSI Design

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Draw the different fabrication step of n-well CMOS? [8]

(b) Derive the V-I characteristics of enhancement MOSFET- [8]

(i) For ohmic Region

(ii) For saturation Region

OR

Q.1 (a) How the V-I characteristic modify with channel length modulation effect? Show its a V-I characteristics and V-I relation. [8]

(b) Draw the transfer conductance characteristic of - [8]

(i) NMOS depletion mode MOSFET

(ii) PMOS enhancement mode MOSFET

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UNIT- II

Q.2 (a) How the threshold voltage V_{To} depends on- [8]

(i) V_{DS}

(ii) V_{SB}

(b) If channel width W = 8 μm, Channel length ℓ = 0.5 μm and is made in a process where process conductivity is 180 μA/V2, Vth = 0.7V and VDD = 3.3V, find The Linearized resistance. [8]

OR

Q.2 (a) What is Noise margin? Explain the procedure to determine noise margin. [8]

(b) What is Body Effect? [8]

UNIT- III

Q.3 (a) Explain power dissipation in the CMOS logic circuit. [8]

(b) Draw two input multiplexer circuit using transmission gate. [8]

OR

Q.3 (a) Explain gate delay for depletion mode inverter. [8]

(b) Provide CMOS logic structure at transistor level for the function: [8]

$$F = \overline{A \cdot (B + C) + D \cdot E}$$

UNIT- IV

Q.4 Draw the stick diagram layout for:

(a) 2 – input CMOS NAND gate [8]

(b) 2 – input CMOS NOR gate [8]

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OR

Q.4 (a) Draw the physical layout for [8]

$$X = \overline{ab + cd}$$

(b) Write a short note on layout optimization? [8]

UNIT- V

Q.5 Write a VHDL code on:

(a) D flip – flop [4]

(b) T flip - flop [4]

(c) J – K flip - flop [4]

(d) S – R flip - flop [4]

OR

Q.5 Write VHDL code for-

(a) 4 – bit adder using full adder [8]

(b) 8:1 MUX [8]

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7E7081

Roll No. _____ Total No of Pages: 3

7E7081

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC1A Antenna & Wave Propagation

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the following terms – [8]

(i) Polarization

(ii) Antenna Temperature

(iii) Isotropic Radiator

(iv) Gain of an Antenna

(b) Derive an expression of Radiated power and Radiation Resistance of a Hertzian dipole. [8]

OR

Q.1 (a) Describe the Beam width and Directivity of an Antenna. [8]

(b) A thin dipole antenna is $\frac{t}{15}$ long. If its loss resistance is 1.5Ω, find radiation resistance and efficiency. [8]

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UNIT- II

Q.2 (a) Calculate the field strength of a uniform linear array. [8]

(b) What is multiplication of patterns? Example with suitable examples. [8]

OR

Q.2 (a) Prove that the directivity of an end-Fire array of the point source spaced at a distance apart is given by – [8]

$$D(\theta) = \frac{2}{1 + \frac{\sin 2\beta d}{2\beta d}}$$

(b) If the phase difference $\delta = -90°$, A uniform linear array consists of 16 isotropic point sources with a spacing of $\frac{\lambda}{4}$, calculate: [8]

(i) Directivity

(ii) Effective aperture

UNIT- III

Q.3 (a) Write short notes on Yagi – Uda antenna and Helical antenna. [8]

(b) Briefly explain Microstrip patch antenna and reflector antenna. [8]

OR

Q.3 (a) Explain the method of Antenna Radiation Pattern measurements. [8]

(b) Explain the working of a folded dipole antenna. [4]

(c) What are the different types of antennas used at very high frequencies? [4]

UNIT- IV

Q.4 (a) Explain the mechanism of Radio wave propagation. [8]

(b) What do you understand by Duct propagation? How are ducts formed? What are its merits and demerits? [8]

OR

Q.4 (a) What is Tropospheric scattering? What are the frequency range for it? [4]

(b) What are the factors affecting space wave field strength? [4]

(c) Derive an expression of field strength due to space wave. [8]

UNIT- V

Q.5 (a) Derive the expression for the Refractive Index of the Ionosphere. [8]

(b) Discuss the characteristics of different ionosphere layers in brief. [8]

OR

Q.5 (a) Explain the effect of Faraday rotation and Earth's magnetic field on Ionospheric wave propagation. [8]

(b) Explain the following in brief – [8]

(i) Skip distance

(ii) MUF

(iii) Virtual height

(iv) Critical Frequency

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7E7078

Roll No. _____ Total No of Pages: 3

7E7078

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. – 2018
Electronic Instrumentation & Control Engineering
7EI3A Digital Image Processing
Common with EC, EIC

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain Image sensing and Acquisition. [8]

(b) What do you mean by Image registration? Describe briefly. [8]

OR

Q.1 What is Colour model or Colour system? Explain RGB, CMY and HSI colour model. [16]

UNIT- II

Q.2 (a) Explain Image smoothing using frequency domain fitters. [8]

(b) What is Spatial Filtering? Define spatial correlation and convolution with an example. [8]

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OR

Q.2 (a) What is Image Sharpening? Explain first and second order derivatives of image sharpening? [10]

(b) Explain Histogram equalization of an image. [6]

UNIT- III

Q.3 Write a short note on –

(a) Inverse filtering [8]

(b) Wiener filtering [8]

OR

Q.3 (a) Explain Image Degradation / Restoration Model in brief. [8]

(b) Explain Erlong (Gamma) Noise and Rayleigh Noise. [8]

UNIT- IV

Q.4 Write a short note on –

(a) Erosion [8]

(b) Dilation [8]

OR

Q.4 (a) What do you mean by gray scale Morphology? [8]

(b) What is Thinning and Pruning? Explain briefly. [8]

UNIT- V

Q.5 (a) What is Watersheds Transformation and construction of Watershed line or Dams? [12]

(b) What do you mean by Image Thresholding? [4]

OR

Q.5 (a) Explain briefly loss – less predictive image compression Technique/ Coding. [12]

(b) Explain basic Image segmentation operations. [4]

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7E7083

Roll No. _____ Total No of Pages: 3

7E7083

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC4A Wireless Communication

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the DSSS with binary phase shift keying and compare its performance with FHSS. [8]

(b) What do you mean by Code division multiplexing? [8]

OR

Q.1 Write short note on -

(a) FHSS signals [8]

(b) Spreading Codes [8]

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UNIT- II

Q.2 (a) What is Link engineering? Explain different types of link used in communication system. [8]

(b) Explain the concept of diffraction loss as a function of path difference around an obstruction by Fresnel zones. [8]

OR

Q.2 (a) What is Multipath fading? Explain various fading channels present. [8]

(b) Explain the transmitter and receiver block diagram of microware link. [8]

UNIT- III

Q.3 (a) Explain the CDMA principle of operation with its advantages and disadvantages. Which type of Handoffs occur in CDMA mobile system? [10]

(b) If a normal GSM time slot consists of 6 trailing bits, 8.25 guard bits, 26 training bits and 2 traffic bursts of 61 bits of data, find the frame efficiency. [6]

OR

Q.3 (a) The "near – far interference" is a serious problem in wireless cellular CDMA network, what is the reason for it? [8]

(b) Explain the TDMA principle of operation with TDMA/TDD example, also write its advantages, disadvantages and efficiency. [8]

UNIT- IV

Q.4 (a) Explain the Process of Speech Coding in GSM. [8]

(b) Write short note on - [4×2=8]

(i) Mobile IP

(ii) Broad band wireless 1002.16

OR

Q.4 (a) Explain the operation of DECT with its network architecture. [8]

(b) Write short note on – [4×2=8]

(i) Zig bee

(ii) RFID Technology

UNIT- V

Q.5 (a) Explain the AOCS and TTC with suitable diagram for a satellite. [8]

(b) Define Satellite access. Describe the difference between single and multiple access. [8]

OR

Q.5 (a) List the main components of an earth station transmitter. With the assistance of a block diagram briefly explain its function of operation. [8]

(b) Write short note on –

(i) Orbital period and Velocity [4]

(ii) High power amplifier [4]

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7E7084

Roll No. _____ Total No of Pages: 3

7E7084

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) What are different kinds of MOS transistors? Explain the structure and operation of MOS transistor. [8]

(b) The process parameters for an NMOS are - [8]

Oxide thickness = 500 A° , Substrate doping $M_A = 10^{16}/cm^3$, Polysilicon gate doping $M_D = 10^{20}/cm^3$, Oxide interface fixed charge density = $2\times10^{10}/cm^3$. Calculate the threshold voltage V_T.

OR

Q.1 (a) What are the different techniques of CMOS transistor fabrication? Explain one in detail. [8]

(b) Explain "Depletion mode MOSFET". [8]

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UNIT- II

Q.2 (a) Write short note on – [8]

(i) Noise Margins

(ii) Pull-up to pull – down ratio for an NMOS inverter.

(b) Design a resistive load inverter with R = 1kΩ such that at V_{OL} = 0.6V. The enhancement type NMOS driver transistor has following parameters : V_{DD} = 5V, V_T = 1V, $\mu_n.C_{ox}$ = 22μ A/V^2 – [8]

(i) Determine the aspect ratio

(ii) Determine Noise margins NM_L and NM_H.

OR

Q.2 (a) Derive β_n/β_p ratio of CMOS inverter. [10]

(b) The NMOS device with V_t = 0.7V has its source terminal grounded and a 1.3V is applied to gate. The device has $\mu_n.C_{ox}$ = 100 mA/V^2, W = 10mm, L = 1mm. Find the value of drain current for V_D = 3V. [6]

UNIT- III

Q.3 (a) Realize the following expression using CMOS inverter – [8]

(i) $AB + \overline{A}\,\overline{B}$

(ii) $\overline{A + BC + DE}$

(iii) AB + BC + AC

(iv) A⊙B

(b) What are DRC rules for layout? State any six DRC rules. [8]

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OR

Q.3 (a) Draw the layout using Euler path for $y = \overline{(A+BC)(D+E)}$. [8]

(b) Draw latch – up formation in CMOS inverter. [8]

UNIT- IV

Q.4 (a) What is C^2 MOS logic? Draw logic circuit using it. What are advantages of such logic? [8]

(b) Explain the working of SRAM cell and DRAM cell. [8]

OR

Q.4 (a) Explain pre – charge and evaluation logic. [8]

(b) Draw $y = \overline{(AB+C)}$ using Domino logic. [8]

UNIT- V

Q.5 (a) Write VHDL Code for S – R flip flop and D-flip flop. [10]

(b) List the advantages and limitations of VHDL. [6]

OR

Q.5 (a) Write the difference between FPGA and custom design. [8]

(b) Write the difference between first and back end design. [8]

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7E7085

Roll No. _____ Total No of Pages: 3

7E7085

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronic Instrumentation & Control Engineering
7EI6.2A/7EC6.1A Advanced Microprocessors
Common with EC, EIC

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the architecture of 8086 with the help of diagram. [8]

(b) List out various flag register bits and their description. [8]

OR

Q.1 (a) Construct minimum mode and maximum mode operation in 8086. [8]

(b) Explain system Bus Timing, and execution of program concept for 8086. [8]

UNIT- II

Q.2 What do you understand by addressing mode? Explain different addressing modes with suitable example for 8086 microprocessor. [16]

OR

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Q.2 (a) Explain with example - [8]

(i) Strings

(ii) Procedures and Macros

(b) Explain Assembler Directives and operators. [8]

UNIT- III

Q.3 Explain various programming mode of 8279 keyboard and display controller. Also draw a block diagram showing its interfacing with microprocessor. [16]

OR

Q.3 Write short note on -

(a) RS – 232 [5]

(b) IEEE – 488 [5]

(c) 8086 based process control system [6]

UNIT- IV

Q.4 (a) Explain memory interfacing and decoding. [8]

(b) Explain DMA controller. [8]

OR

Q.4 (a) Explain interfacing microprocessor to keyboard and alpha numeric displays. [10]

(b) Compare static memory and dynamic memory. [6]

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UNIT- V

Q.5 (a) Explain multi user operating system concepts. [8]

(b) Explain 8086 based multiprocessor systems. [8]

OR

Q.5 Write short note on -

(a) 286 processors [4]

(b) 386 processors [4]

(c) 486 processors [4]

(d) Pentium processors [4]

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7E7086

Roll No. _____ Total No of Pages: 3

7E7086

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. – 2018
Electronics & Communication Engineering
7EC6.3A VHDL

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Describe the programming structure of VHDL and also explain Functional Simulation. [8]

(b) Describe the Behavioral & Structural style of modeling with suitable example. [8]

OR

Q.1 Write a VHDL code for -

(a) D – Latch. [4]

(b) Half adder [4]

(c) 4 × 1 MUX [4]

(d) 3 - input NAND gate [4]

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UNIT- II

Q.2 (a) Explain Sequential statements with example. [8]

(b) VHDL Description of structure with suitable example? [8]

OR

Q.2 (a) Given the following function f = ab + cd. Write an entity declaration and alternative architectures for a system that computes the function. [8]

(b) Explain Model Organization with example. [4]

(c) What is NULL Transactions? Explain. [4]

UNIT- III

Q.3 (a) Consider the function: $y = \overline{x_1}\,\overline{x_3} + x_2\,\overline{x_3} + \overline{x_1}\,x_2$. Use the truth table to derive a circuit for y that uses a 2 – to – 1 MUX. [8]

(b) Write a VHDL Code that specifies the barrel shifter circuit. [8]

OR

Q.3 (a) Explain in brief Binary encoder & Binary decoder and explain Sensitivity list. [8]

(b) Write a VHDL Code for a BCD – to – 7 Segment Code converter using a select signal assignment. [8]

UNIT- IV

Q.4 (a) Write a VHDL Code of Serial Adder and also explain one hot encoding. [8]

(b) Write short note on Mealy type FSM with example. [8]

OR

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Q.4 (a) Write down short note on Vending Machine with example. [8]

(b) Write down VHDL Code for Moore type FSM and also be explain Mealy type finite state machine. [8]

UNIT- V

Q.5 (a) How many 16K memories can be placed (without over lapping) in the memory space of a processor that has 24 address lines? [8]

(b) Using Logic gates, design an active low chip select for the memory device described in each of the following situations. [8]

OR

Q.5 (a) Explain SRAM in brief and what is Clock skew and how it can be minimized? [8]

(b) Write a VHDL Code for Sorting operation and Multiplier. [8]

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7E7071

Roll No. _____ Total No of Pages: 2

7E7071

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronic Instrumentation & Control Engineering
7E11A Neural Networks and Fuzzy Logic Control

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 Explain the followings -

(a) Neurophysiology [8]

(b) Difference between biological neural network and artificial neural network. [8]

OR

Q.1 (a) Explain the McCulloch-Pitts model? [8]

(b) Explain the limitations of single layered neural network. [8]

UNIT- II

Q.2 Explain the "Adaline" in detail. [16]

OR

Q.2 Explain the followings -

(a) Back propagation learning Law [8]

(b) Supervised learning [8]

SY2

UNIT- III

Q.3 Explain all features of Membership functions. [16]

OR

Q.3 Explain the followings –

(a) Uncertainty and precision [8]

(b) Maximum membership principal [8]

UNIT- IV

Q.4 Explain all the Defuzzification methods in detail with suitable examples. [16]

OR

Q.4 Explain the followings –

(a) Graphical techniques of reference [8]

(b) Neural languages, Linguistic Hedges and rule based system [8]

UNIT- V

Q.5 Explain the General Fuzzy logic controller with a neat sketch and suitable examples. [16]

OR

Q.5 Explain –

(a) Fuzzy MIMO system [8]

(b) Fuzzy statistical process control [8]

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7E7072

Roll No. _____

Total No of Pages: 4

7E7072

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronics & Communication Engineering
7E12A Digital Signal Processing
Common with AI, EC, EIC

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. NIL

UNIT- I

Q.1 (a) Determine the Nyquist rate & Nyquist interval for the following signal –

$$x(t) = \frac{1}{\pi t} \sin(600\pi t)$$ [6]

(b) Draw block diagram of continuous time processing of discrete time signals and write mathematical expression in term of time domain and frequency domain for output of each stage. [10]

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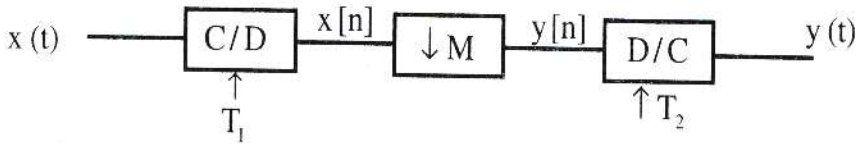
OR

Q.1 Consider the system in figure – [16]



Assume that the input is band limited :

$$x_c(jw) = 0 \quad \text{for} \; |W| > 2\pi.1000$$

(a) What constraint must be placed on M_1T_1 & T_2 in order for ya (t) to be equal to xa (t)?

(b) If $f_1 = f_2 = 20$ KHz & M = 4, find the expression for ya (t) in terms of xa (t).

UNIT- II

Q.2 (a) Determine the homogeneous solution of the system, described by – [8]

$$y(n) - 3y(n-1) - 4y(n-2) = x(n)$$

(b) $H(z) = \dfrac{1+3z^{-1}}{1+\frac{1}{2}z^{-1}}$, write an expression of inverse system of H(z). [8]

OR

Q.2 (a) Define Minimum – phase system, write –

(i) Generalized expression of minimum – phase. [4]

(ii) Discuss stability and causality condition for a discrete system. [4]

(b) Write short notes on the following –

(i) All – pass system [4]

(ii) Frequency response of LTI system [4]

UNIT- III

Q.3 (a) Obtain direct form I and II realization of a system described by – [10]

$$y(n) - \frac{3}{4} y(n-1) + \frac{1}{8} y(n-2) = x(n) + \frac{1}{2} x(n-1)$$

(b) Realize the system with difference equation – [6]

$$y(n) = \frac{3}{4} y(n-1) - \frac{1}{8} y(n-2) + x(n) + \frac{1}{3} x(n-1)$$

in cascade form.

OR

Q.3 (a) Draw the cascades and parallel realizations for the following system functions - [10]

$$H(z) = \frac{1 + \frac{1}{4} z^{-1}}{\left(1 + \frac{1}{2} z^{-1}\right)\left(1 + \frac{1}{2} z^{-1} + \frac{1}{4} z^{-2}\right)}$$

(b) Explain the FIR system and Transposed form. [6]

UNIT- IV

Q.4 Design an FIR linear phase filter using Kaiser Window to meet the following specification – [16]

$0.99 \leq |H(e^{jw})| \leq 1.01$, for $0 \leq |w| \leq 0.19\pi$

$|H(e^{jw})| \leq 0.01$, for $0.21\pi \leq |w| \leq \pi$

OR

Q.4 Write short notes on the following –

(a) Bilinear transformation [8]

(b) Impulse invariance transformation [8]

UNIT- V

Q.5 Explain the following –

(a) Decimation in Time FFT Algorithm [10]

(b) Properties of the DFT [6]

OR

Q.5 Determine the four point DFT of the sequence x(n) = (1, 0, 2, 1) using DIT Algorithm. [16]

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7E7073

Roll No. _____ Total No of Pages: 2

7E7073

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronic Instrumentation & Control Engineering
7E14A Analytical & Environmental Instrumentation

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Explain the principle of atomic absorption spectrophotometer. Discuss its working with functional block diagram. [3+5=8]

(b) How mass spectroscopy is different from optical spectroscopy. Describe the components of a mass spectrometer. [3+5=8]

OR

Q.1 (a) Explain the principle of fluorescence spectroscopy. Discuss the working of a double beam fluorimeter with a schematic diagram. [3+5=8]

(b) Discuss the following with reference to X-ray spectrometry: [2×4=8]

(i) X-ray generation

(ii) Collimator

(iii) Monochromators

(iv) Detectors.

UNIT- II

Q.2 (a) Discuss the working principle of conventional infrared gas analyzers. List its drawbacks and how these are overcome in improved infrared gas analyzer. [5+3=8]

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(b) Explain the working of thermal conductivity gas analyzers and discuss working of hot wire thermal conductivity gas analyzer. [3+5=8]

OR

Q.2 (a) Discuss a scheme for measurement of CO_2 in flowing beverage used infrared gas analyzers. [8]

(b) Explain the working of chemiluminescent ozone analyzer with a functional block diagram. [8]

UNIT- III

Q.3 (a) Explain the working principle of Gas chromatograph. Discuss the applications. [8]

(b) Explain the working of high pressure liquid chromatography with schematic diagram. [8]

OR

Q.3 (a) Discuss the working of any two detectors used in gas chromatographs. [8]

(b) Discuss with reference to liquid chromatography.

(i) Sample injection system [4]

(ii) Detection system [4]

UNIT- IV

Q.4 (a) What are the major effects of the Sulphur oxide pollutants? Discuss a conductivity method of measurement of SO_2 in air. [3+5=8]

(b) How Nitrogen oxides affects the environment. Explain the measurement technique of nitrogen oxides using CO Laser. [3+5=8]

OR

Q.4 (a) Discuss the working principle of measurement of hydrocarbons by flame ionization detection technique. [8]

(b) Explain the following:-

(i) Smoke monitor [4]

(ii) Visible emission monitoring system [4]

UNIT- V

Q.5 (a) What is pH? Explain the principle of pH measurement. [3+5=8]

(b) What is meant by ion selective electrodes? Discuss its types, merits and de-merits. [3+5=8]

OR

Q.5 (a) Explain the basic principle of conductivity meters. Discuss the measurement of conductance by Null method. [3+5=8].

(b) Explain the working principle of analyzer for measurement of dissolved oxygen. [8]

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7E7074

Roll No. _____ Total No of Pages: 2

7E7074

B. Tech. VII Sem. (Main / Back) Exam., Nov. – Dec. - 2018
Electronic Instrumentation & Control Engineering
7E15A Instrumentation in Industries

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks: 26

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT- I

Q.1 (a) Draw and explain the man power distribution curve for process industries. [8]

(b) Explain instrument department functions and responsibilities with the help of organizational chart in process plant instrumentation. [8]

OR

Q.1 (a) What are the various control panels and displays are used in process industries? Explain in brief. [8]

(b) Why power plant training is useful for instrumentation engineer? Discuss about the major areas of power plant training for process Industries. [8]

UNIT- II

Q.2 (a) Draw and explain the C & I diagram of cascade temperature control with heating & cooling capability. [8]

(b) Draw and explain the C & I diagram of Reactor pressure control by throttling flow of vent gas. [8]

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OR

Q.2 (a) Explain the control schemes of Reactor pressure control by modulating gas make up. [8]

(b) Discuss about the C & I of Reactor temperature control with recirculation. [8]

UNIT- III

Q.3 (a) Explain the control schemes of steam trap replaced by level control. [8]

(b) Explain the C & I of Temperature pressure cascade control loop on steam heater. [8]

OR

Q.3 Explain the following –

(a) Condenser control by changing the wetted surface area. [8]

(b) Hot gas by pass control of Heat exchangers. [8]

UNIT- IV

Q.4 (a) Explain the principles and classification of dryers with neat sketches. [8]

(b) Explain the C & I diagram of forced circulation type evaporators with merits & demerits. [8]

OR

Q.4 Explain the following C & I diagrams –

(a) C & I of throttling control of rotary pumps. [8]

(b) Heated cylinder type dryer control schemes. [8]

UNIT- V

Q.5 (a) Explain the instrumentation & control schemes of feed water control for a boiler. Also, explain safety interlocks associated with it. [8]

(b) What are the selection criteria of instrumentation for steam power plants? Explain the different factors consideration for designing the control room of steam power plants. [8]

OR

Q.5 Write short notes on –

(a) Data logging & computing equipments in steam power plants. [8]

(b) Air – Fuel ratio control in combustion unit of power plants. [8]
