7E7076

Roll No. ____________ Total No of Pages: 3

7E7076
B. Tech. VII Sem. (Main) Exam., Nov.-Dec.-2016
Electronic Instrumentation & Control Engineering
7EI6.2A Advanced Microprocessor
EC, EIC

Time: 3 Hours | **Maximum Marks: 80**
Min. Passing Marks-Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain Internal Architecture of 8086 microprocessor. [8]

(b) What is minimum and maximum mode of 8086 microprocessor? Explain Interfacing of minimum and maximum modes. [8]

OR

Q.1 (a) Explain PIN diagram of 8086 microprocessor. [8]

(b) Explain classification of Registers in 8086 Microprocessor. [8]

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UNIT – II

Q.2 (a) Explain addressing modes of 8086 microprocessor. [8]

(b) Explain the following instruction with examples -

(i) LES [2]

(ii) CBW [2]

(iii) MUL [2]

(iv) AAA [2]

OR

Q.2 (a) Explain classification of Interrupts [8]

(b) Write short note on-

(i) Procedure [2]

(ii) Assembles Directive [3]

(iii) Macros [3]

UNIT – III

Q.3 (a) Explain Interfacing of A/D converter. [8]

(b) Write short note on-

(i) RS – 232 [4]

(ii) IEEE 488 [4]

OR

Q.3 (a) Explain Interfacing a microprocessor to keyboards. [8]

(b) Write Short Note on "8086 based process control system. [8]

UNIT – IV

Q.4 (a) Explain Interfacing of Microprocessor to alphanumeric display. [8]

(b) Explain DMA controller in 8086 Microprocessor with pin diagram. [8]

OR

Q.4 Write Short Note on-

(i) Memory Interfacing and Decoding [8]

(ii) Programmable Parallel Ports [8]

UNIT – V

Q.5 Explain following Multiprocessor configuration-

(i) Coprocessor [6]

(ii) Closely coupled [6]

(iii) Loosely coupled [4]

With block diagram of each configuration.

OR

Q.5 Write the features and also explain the architecture of following processor-

(i) 80386 [8]

(ii) 80286 [8]

7E7078

Roll No. ____________ Total No of Pages: 2

7E7078

B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016
Instrumentation Control Engineering
7EC3A Digital Image Processing

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

Q.1 (a) What are the basic components of a digital image processing system? Write down the three examples of field that use digital image processing. [8]

(b) Explain the basic concepts in sampling and quantization digital image processing. [8]

OR

Q.1 Explain all the elements of visual perception light and electromagnetic spectrum. [16]

UNIT - II

Q.2 (a) Explain why the discrete histogram equalization technique does not, in general, yield a flat histogram. [8]

(b) Discuss the limiting effect of repeatedly Appling a 3×3 low pass spatial filter to a digital image. You may ignore border effect. [8]

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OR

Q.2 Describes the various types of frequency domain filters. [16]

UNIT – III

Q.3 What is digital image restoration process? Explain noise probability density function. [16]

OR

Q.3 (a) Explain the adaptive median filter and also write application. [8]

(b) Explain the noise estimation parameter. [8]

UNIT – IV

Q.4 Explain the Hit-or-Miss transformation. How can we remove the noise from image by opening and closing morphological operation. [16]

OR

Q.4 Explain following: - [16]

(a) Convex Hull

(b) Thickening

(c) Skeletons

(d) Pruning

UNIT – V

Q.5 Discuss fundamentals of digital image compression and scaling methodologies. [16]

OR

Q.5 Explain the fundamental of edge – based segmentation. [16]

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7E7081

Roll No. ________ Total No of Pages: 3

7E7081

B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electronics &Communication Engineering
7EC1A Antenna & Wave Propagation

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main : 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit.** All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) A transmitting antenna carries current of 20 A (rms) at a frequency of 170 kHz and produces a field strength of 1.8 mV/m at a distance of 20 km. Estimate the effective height of the antenna. [8]

(b) Define the following terms:- [2×4=8]

(i) Isotropic radiator

(ii) Beam width of an antenna

(iii) Directivity of an antenna

(iv) Gain of an antenna

OR

Q.1 (a) A thin dipole antenna is t/15 long. If its loss resistance is 1.5 Ω, find radiation resistance and the efficiency. [4×2=8]

(b) Write short note on: - [4×2=8]

(i) Antenna Temperature

(ii) Polarization

UNIT – II

Q.2 (a) For a end five array consisting of several half wave length long isotropic radiators is to have a directive gain of 30. Find the array length and width of the major lobe (i. e. beam width between first nulls). What will be these for a broadside array? [8]

(b) Explain the principles of End-five and broadside arrays. [8]

OR

Q.2 (a) A Uniform linear array consists of 16 isotropic point sources with a spacing of $\lambda/4$. If the phase difference $\delta = -90°$, calculate - [2×4=8]

(i) HPBW

(ii) Beam solid angle

(iii) Directivity

(iv) Effective aperture.

(b) Prove that the directivity of an end five array of the point source spaced at a distance apart is given by [8]

$$D(\theta) = \frac{2}{1 + \frac{\sin 2\beta d}{2\beta d}}$$

UNIT – III

Q.3 (a) What are the different types of antennas used at very high frequencies? Explain the working of a folded dipole antenna. [8]

(b) Find out the beam width between first nulls and power gain of a 2m paraboloid reflector operating at 6000 MHz. [8]

OR

Q.3 (a) Explain with suitable diagrams the working of the log periodic antenna. What are the practical applications of these antennas? [8]

(b) Write short note on :- [4×2=8]

(i) Helical antenna

(ii) Yagi - uda antenna.

UNIT – IV

Q.4 (a) Explain the mechanism of radio wave propagation. [8]

(b) What is tropospheric scattering? What are the frequency ranges for it? Why are such ranges only applicable for tropospheric scattering? [8]

OR

Q.4 (a) What do you understand duct propagation? How are ducts formed? What are its merits, advantages and limitations? [8]

(b) If h_t and h_r are the heights in meters of transmitting and receiving antennas above the ground, show that maximum separation between them for line of sight transmission is $D_{max} = 3.57\left[\sqrt{h_t} + \sqrt{h_r}\right]$km [8]

UNIT – V

Q.5 (a) Derive the expression for the Refracting Index of the Ionosphere. [8]

(b) At what frequency a wave must propagate for the Dregion to have an index of refraction 0.6. Given N = 300 election/cm^3 for Dregion. [8]

OR

Q.5 (a) Explain the effects of earth's magnetic field on ionospheric wave propagation. [8]

(b) F_2 layer of the ionosphere has an electron density of 0.81×10^{12} per M^3 at a height of 350 km from the earth's surface. Find the critical frequency of this layer. Also find the maximum usable frequency between two stations 1500 kms apart. Neglect earth's curvature. [8]

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7E7083	Roll No. __________	Total No of Pages: 3

7E7083
B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electronics &Communication Engineering
7EC4A Wireless Communication

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main : 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

Q.1 (a) Explain the DSSS with binary phase shift keying and compare its performance with FHSS. [8]

(b) If the chip rate of a DSSS transmitter is 20Mbps, the message bit rate is 10 kbps. Find out the processing gain achieved, if bpsk is used. [6]

(c) Write the properties of PN sequence. [2]

OR

Q.1 (a) Explain FHSS with basic block diagram and find the expression for processing gain (Gp) in fast and show systems. [8]

(b) Explain the properties of spreading codes. How they are generated? Briefly explain. [8]

UNIT – II

Q.2 (a) Explain small scale fading and write the time dispersion parameters. [8]

(b) Assume a receiver is located 20 km from a 100 W transmitter. The carrier frequency is 1000 MHz, free space propagation is assumed. Gy = 1 and Gr = 3. Find the power at receiver. [8]

OR

Q.2 (a) Explain the concept of diffraction loss as a function of path difference around an obstruction by Fresnel zones. [8]

(b) Explain the transmitter and receiver block diagram of Microwave link. [8]

UNIT – III

Q.3 (a) The "near – far interference" is a serious problem in a wireless cellular CDMA network, what is the reason for it? [8]

(b) What is rake receiver? [4]

(c) What is soft Hand off? [4]

OR

Q.3 (a) Define briefly the operation of a time division multiple access (TDMA) schemes. [8]

(b) Compare FDMA, CDMA & TDMA. [8]

UNIT – IV

Q.4 (a) Explain the process of speech coding in GSM. [6]

(b) Define Hand off and Handovers in GSM. [6]

(c) Compare WiFi and WiMax Technology. [4]

OR

Q.4 (a) Explain RFID Technology. [6]

(b) Explain briefly:

(i) Bluetooth [5]

(ii) Broadband wireless 1002.16 [5]

UNIT – V

Q.5 Write short note on following:

(a) Low noise amplifier [4]

(b) Up converter [4]

(c) Down converter [4]

(d) Monitoring and control [4]

OR

Q.5 (a) Explain the process of Link Design of a satellite system and derive an expression for the received power. [8]

(b) Define following:

(i) Coverage angle [2]

(ii) Slant range [2]

(iii) Orbital period [2]

(iv) Orbital velocity [2]

7E7084

Roll No. ____________ Total No of Pages: 4

7E7084
B. Tech. VII Sem. (Main) Exam., Nov.-Dec.-2016
Electronics & Communication Engineering
7EC5A VLSI Design

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) The Process Parameters for an NMOS are

oxide thickness $t_{ox} = 500A°$

substrate doping $M_A = 10^{16} /cm^{+3}$

Polysilicon gate doping $M_D = 10^{20} / cm^3$

Oxide interface fixed charge density = $2 \times 10^{10}/cm^3$.

Calculate the Threshold Voltage V_T for it. [10]

(b) Discuss following High order effects in MOSFET -

(i) narrow channel effect [3]

(ii) sub threshold conduction [3]

OR

Q.1 (a) Draw all fabrication steps to achieve following inverter (fig. 1) [8]

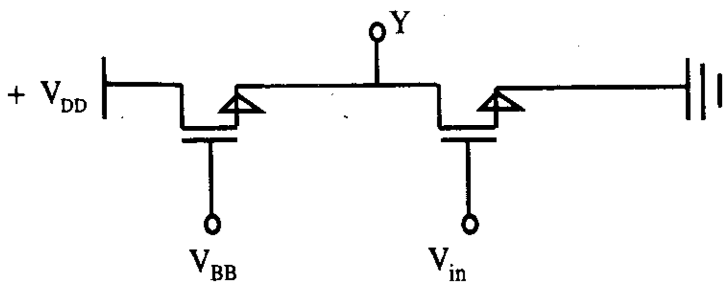

Fig – 1

Starts the fabrication using n – type substrate.

(b) Calculate the Junction capacitance at drain end in a NMOS shown in fig – 2 [8]

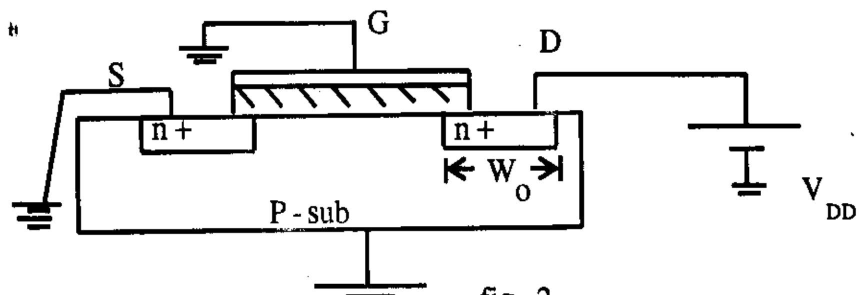

fig - 2

With substrate doping $N_A = 10^{12} / cm^3$

drain doping $N_D = 10^{18} / cm^3$

Junction depth $X_j = 0.1km.$

Drain Pellet is square of size $w_o \times w_o = (0.01 \times 0.01)\ km^2$

UNIT – II

Q.2 (a) Define noise margin for low and noise margin for high. Calculate these value for a CMOS inverter having $V_{tn} = |V_{tp}| = 0.8$, $\frac{Kn}{Kp} = 2.5$, and supply is $V_{DD} = 5$ volt. [8]

(b) Draw CMOS logic circuit for realize $y = \overline{[A(B+C)]\ (DEE)} = \overline{ADE\ (B+C)}$. Also set the (W/L) of each NMOS and PMOS such that the equivalent ratio of $\frac{Kn}{Kp} = 4$. [8]

OR

Q.2 (a) Draw the edge triggered D – Latch using CMOS logic. [6]

(b) Draw 4×1 Mux using transmission gate. Also compare the total no. of transistor required for such Mux using CMOS and TG. [6]

(c) Define power delay product (PDP) and energy delay product (EDP). Discuss why these parameters are called Figure of Merit for logic circuit. [4]

UNIT – III

Q.3 (a) Draw the Layout using possible Euler path for $y = \overline{(A+BC)\ (D+E)}$ [8]

(b) Draw the 2 × 1 Mux Layout using TG. [8]

OR

Q.3 (a) What are DRC rules for Layout? State any six DRC rules. Why we need to follow DRC rules when draw layout for any logic circuit? [6]

(b) Draw the Layout for a Half Adder using CMOS logic. [6]

(c) Draw Latch – up formation in CMOS inverter. [4]

UNIT – IV

Q.4 Draw following & explain their working- [4×4=16]

(a) SRAM cell

(b) DRAM cell

(c) $y = \overline{(AB + C)}$ using Domino logic

(d) Any NP (zipper) logic

OR

Q.4 (a) Explain the pre-charge and evaluation logic and explain zero transfer in detail. [8]

(b) What is C^2MOS logic? Draw any logic circuit using it. What are additional advantages of such logic? [8]

UNIT – V

Q.5 (a) Write the difference between custom design and FPGA in respect of design time and cost. [8]

(b) Write VHDL code for 2 input NAND and NOR gate. [8]

OR

Q.5 Write short note on any two - [2×8=16]

(i) ASIC Design

(ii) VHDL code for FF

(iii) Difference between First and Back End design.

7E7086

Roll No. ____________ Total No of Pages: 3

7E7086
B. Tech. VII Sem. (Main) Exam., Nov.-Dec.-2016
Electronics &Communication Engineering
7EC6.3A VHDL

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main : 26

Min. Passing Marks Back: 24

Instructions to Candidates:

Attempt any five ***questions,*** *selecting one* ***question*** *from* ***each unit.*** *All questions carry* ***equal*** *marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 Describe the following in VHDL based design - [4×4=16]

(i) Functional simulation

(ii) Logic synthesis

(iii) Place and route

(iv) Timing simulation

OR

Q.1 (a) Write important features of HDLs which are not common to conventional high – level programming languages. [8]

(b) What is a UUT? What are the primary advantages of using a testbench for simulation rather than performing an interactive and/ or a command – line – driven simulation? [8]

UNIT – II

Q.2 (a) List the three steps an event driven – simulator performs to accomplish a simulation. [8]

(b) Given the following architecture body. [8]

```
architecture mixed of fcn is
signal s1, s2 : std_logic;
begin
u0 : s1 <= '1' when a = '0' and b = '1' else '0';
u1 : with std_ logic _ vector' (a, c) select
s2 <= '1' when "11",
'0' when others;
u2 : process (s1, s2)
begin
f < = s1 or s2;
end process;
end mixed;
```

(i) Write the entity declaration for the given architecture.

(ii) Write each of the simulation processes created by elaboration.

(iii) Assuming a testbench contains a process tb, which applies all possible input values and verifies the output, draw a diagram of the simulation net. Assume that the instantiation of the design entity in the test bench is labeled uut.

OR

Q.2 (a) Given the following function: f = a + bc [8]

Write an entity declaration and three alternative architectures for a system that computes the function.

(b) Explain states of simulation process. [4]

(c) Write key differences between signal and variables. [4]

UNIT – III

Q.3 (a) For the function f (w1, w2, w3) = $\sum m$ (0, 2, 3, 6), use shannon's expansion to drive an implementation using a 2-to-1 multiplexer and other necessary gates. [8]

(b) Write VHDL code for implementation of 4×1 mux using 2×1 mux. [8]

OR

Q.3 (a) For the function f (w1, w2, w3) = $\sum m$ (0, 4, 6, 7), use shannon's expansion to drive an implementation using a 2-to-1 multiplexer and other necessary gates. [8]

(b) Write VHDL code for n-bit left – to – right shift register using generic statement. [8]

UNIT – IV

Q.4 (a) Design hardware to implement 11 sequence detector using Mealy type FSM, clearly mentioning the steps for design. [8]

(b) Write VHDL code to implement 11 sequence detector using mealy machine. [8]

OR

Q.4 (a) Design hardware to implement serial adder using Moore type FSM, clearly mention the steps for design. [8]

(b) Write VHDL model for implementation of serial adder using Moore type FSM. [8]

UNIT – V

Q.5 (a) Draw data path and controller ASM chart of the divider circuit. [6]

(b) Write VHDL code for the above divider circuit. [10]

OR

Q.5 (a) Define clock skew. [4]

(b) Write VHDL code for sorting circuit which makes use of kxn synchronous SRAM block. [12]

7E4047

Roll No. ____________ Total No of Pages: 2

7E4047

B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Electronics & Communication Engineering
7EC4 (O) IC Technology

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*
Units of quantities used/calculated must be stated clearly.
Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 What are basic features of float zone growth? Give its advantages & disadvantages. Explain the Top Seed & Bottom Seed process. [16]

OR

Q.1 (a) What are the different types of defects in crystal structure? Explain with diagram. [8]

(b) What are the various steps for wafer preparation? Explain each in detail. [8]

UNIT – II

Q.2 (a) Define Fick's Law of Diffusion. Describe analytic solution used for Fick's Law. [8]

(b) Write short note on oxidation techniques. [8]

OR

Q.2 (a) Explain Deal – Grove model of oxidation. [8]

(b) Write short note on oxide properties. [8]

UNIT – III

Q.3 What do you mean by epitaxy? Explain vapour phase epitaxy and defects in epitaxial growth. [16]

OR

Q.3 (a) Explain chemical equilibrium and law of mass action. [8]

(b) What is Molecular Beam Epitaxy? Give the advantages of molecular beam epitaxy over CVD. [8]

UNIT – IV

Q.4 (a) What is photoresists? Discuss types of photoresists and components of photoresists. [8]

(b) What is optical lithography? Explain proximity printing and compare it with contact and projection printing. [8]

OR

Q.4 (a) Explain the process of masking. [8]

(b) Write technical note on wet etching. [8]

UNIT – V

Q.5 (a) Give an account of applications and desired properties of metallization. [8]

(b) Explain NMOS fabrication process sequence. [8]

OR

Q.5 write short note on:

(a) SOI techniques [8]

(b) Problems associated with metallization. [8]

7E4048

Roll No. __________ Total No of Pages: 3

7E4048

B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Electronics & Communication Engineering
7EC5(O) VLSI Design

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Draw symbolic diagram and internal structure of enhancement type NMOS transistor and explain its working. [6]

(b) Draw input – output characteristics and transfer characteristic of enhancement type NMOS and explain. [6]

(c) Explain using transfer characteristics that how depletion mode operation is preformed in enhancement type MOSFET. [4]

OR

Q.1 (a) Draw and explain CMOS fabrication steps using n-well technology. [8]

(b) Compare N-well, P-well and twin well CMOS fabrication technologies. [8]

UNIT – II

Q.2 (a) Derive $I_{DS} - V_{DS}$ relation for MOS transistor - [10]

(i) without channel length modulation

(ii) with channel length modulation

(b) Draw and explain MOS transistor circuit model. [6]

OR

Q.2 (a) Draw and explain voltage transfer characteristics of CMOS Inverter. Mark various operating regions and operating modes of transistor in these regions. [10]

(b) Write a brief note on body effect of MOS transistor and explain how it affects the noise margin and beta ratio of CMOS inverter. [6]

UNIT – III

Q.3 (a) Mark the advantages of transmission gate over CMOS. Justify the answer using I/O characteristics or transfer characteristics giving suitable example. [12]

(b) Implement 2×1 multiplexer using transmission gate. [4]

OR

Q.3 (a) Implement 2 – Input CMOS NAND gate and NOR gate. Determine the equivalent size of pull-up and pull-down circuit, considering $\left(\frac{W}{L}\right)_n$ as size of NMOS and $\left(\frac{W}{L}\right)_p$ as size of PMOS transistor respectively. [10]

(b) Derive the expression for propagation delay in CMOS inverter. [6]

UNIT – IV

Q.4 (a) Draw layout diagram for 2 – Input CMOS NAND and NOR gates. [8]

(b) Write a brief note on scalable design rules used in CMOS layout design. [8]

OR

Q.4 (a) Implement the following function using CMOS and draw its layout. [8]

$\overline{Y} = \overline{A}B + C$

(b) Write a brief note on MOS layout optimization for performance. [8]

UNIT – V

Q.5 Define the following in VHDL-

(a) Entity [4]

(b) Architecture [4]

(c) Package [4]

(d) Configuration [4]

OR

Q.5 (a) Write VHDL code for D flip – flop in behavioral style – [10]

(i) Level triggered

(ii) Negative edge triggered

(b) Differentiate signal and variable in VHDL. [6]

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7E4051	Roll No. __________ Total No of Pages: 3

7E4051

B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Electronics Communication
7EC6.3 (O) Operating System

Time: 3 Hours | **Maximum Marks: 80**
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL   2. NIL

UNIT – I

Q.1 (a) What are the functions of an operating system? Explain the types of operating systems in brief. [8]

(b) Explain the following: [8]

(i) Kernel level thread

(ii) System call

(iii) Boot strap loader

(vi) Multithreading OS

OR

Q.1 (a) What is a Process? What is the difference between a Program and a Process? Explain PCB using a suitable example. [8]

(b) How an operating system works as a resource manager and vertical machine? [8]

UNIT - II

Q.2 (a) What is Critical Section Problem? Explain the role of lock variable and TSL instruction in busy waiting. [8]

(b) What is the difference between preemptive and non – preemptive scheduling? [4]

(c) Explain the turnaround time and response time. [4]

OR

Q.2 (a) What is dinning philosophers problem? Explain the solution of the problem by using a suitable example. [8]

(b) Consider the following set of processes with arrival time and CPU bust time gives in ms -

Process	Arrival time	Burst time
P_1	0	8
P_2	1	4
P_3	2	9
P_4	3	5

What is the average waiting time for these processes with preemptive SJF Scheduling? [8]

UNIT - III

Q.3 (a) Explain free space management using bit map, linked list, free list. [8]

(b) Consider the following snap shot of the system:- [8]

Process	Allocation			Maximum			Available		
	A	B	C	A	B	C	A	B	C
P_0	0	1	0	7	5	3	3	3	2
P_1	2	0	0	3	2	2			
P_2	3	0	2	9	0	2			
P_3	2	1	1	2	2	2			
P_4	0	0	2	4	3	3			

If a request from process P_1 arrives for (0, 1, 2), can the request be granted immediately? What is the content of need matrix?

OR

Q.3 (a) What is deadlock? What are the necessary conditions to occur the deadlock? What are the various methods to recover from the deadlock? [8]

(b) Explain the difference between logical and physical address space. Explain fragmentation. What are the various solutions for external fragmentation? [8]

UNIT – IV

Q.4 What is virtual memory? Explain the use of virtual memory using a suitable example. [16]

OR

Q.4 (a) What is the difference between pager and swapper? [4]

(b) What is thrashing? [4]

(c) Write short note on TLB. [4]

(d) What is demand paging? [4]

UNIT – V

Q.5 Write shot note on:-

(a) Directory structure in link. [4]

(b) File naming [4]

(c) Acyclic graph [4]

(d) File organization [4]

OR

Q.5 Explain the thread states with diagram and explain how "Threads" approach improves performance of operating system. [16]

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7E7071

7E7071
B. Tech. VII Sem. (Main) Exam., Nov.-Dec.-2016
Electronic Instrumentation & Control Engineering
7EI1A Neural Networks and Fuzzy Logic Control

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main : 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from each **unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain the various differences between artificial and biological Neural Networks. [8]

(b) Explain the McCulloch – Pitts model. [8]

OR

Q.1 Generate the output of logic AND, OR, AND NOT function using McCulloch Pitts neuron. [16]

UNIT – II

Q.2 Four steps of Hebbion learning of a single neuron network as shown in fig. have been implemented starting with $w^1=[1\ -1]^t$ for learning constant C=1 using input as follows:

$$x_1=\begin{bmatrix}1\\-2\end{bmatrix},\ x_2=\begin{bmatrix}0\\1\end{bmatrix},\ x_3=\begin{bmatrix}2\\3\end{bmatrix},\ x_4=\begin{bmatrix}1\\-1\end{bmatrix}.$$

Find final weights for – [16]

(a) Bipolar binary f(net), (b) Bipolar binary continuous f(net)

OR

Q.2 Explain the following-

(a) Back Propagation Learning Law [8]

(b) Widrow – Hoff Learning Algorithm [8]

UNIT – III

Q.3 (a) What is the membership function? Explain all features of membership function. [8]

(b) Differentiate the CRISP sets from fuzzy sets. [8]

OR

Q.3 Explain the following-

(a) Fuzzyfication [8]

(b) Maximum Membership Principle [8]

UNIT – IV

Q.4 Explain the following-

(a) Centroid Method [8]

(b) Weighted Average Method [8]

OR

Q.4 Explain the following-

(a) Graphical techniques of reference [8]

(b) Aggregation of fuzzy rules [8]

UNIT – V

Q.5 Draw & explain the fuzzy control system block diagram. [16]

OR

Q.5 Explain the following-

(a) MIMO Control System [8]

(b) Fuzzy Statistical Process Control System [8]

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Roll No. ____________

Total No of Pages: 2

7E7072

7E7072

B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electronics & Communication Engineering
7EI2A Digital Signal Processing

Time: 3 Hours

Maximum Marks: 80
Min. Passing Marks Main : 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain Energy & Power Signals with help of suitable examples. [8]

(b) Explain Sampling & different types of Sampling Techniques. [8]

OR

Q.1 (a) Explain in detail the concept of continuous time processing of discrete time signals. [8]

(b) Explain the properties & applications of discrete time signals. [8]

UNIT – II

Q.2 (a) For the Transform analysis of LTI System, explain the phenomena of all pass System. [8]

(b) Find the magnitude & phase responses for the system characterized by difference equation - $y(n)=\frac{1}{6}x(n)+\frac{1}{3}x(n-1)+\frac{1}{6}x(n-2)$ [8]

OR

Q.2 (a) Explain Linear System with Linear phase. [8]

(b) Discuss briefly the frequency response of LTI system. [8]

UNIT – III

Q.3 Obtain the structures of cascade & parallel realization of following transfer function - $H(z)=\frac{(1-z^{-1})^3}{\left(1-\frac{1}{2}z^{-1}\right)\left(1-\frac{1}{8}z^{-1}\right)}$ [16]

OR

Q.3 (a) Explain filter & their use in DSP. [8]

(b) Compare the structures for IIR & FIR System. [8]

UNIT – IV

Q.4 (a) For design of FIR filters by windowing, explain Hamming & Kaiser. [8]

(b) Convert the analog filter into a digital filter whose system function is- $H(S)=\frac{S+0.2}{(S+0.2)^2+9}$ Use the impulse invariant technique. Assume T= 1s. [8]

OR

Q.4 (a) Convert the analog filter with system function $H(S)=\frac{S+0.1}{(S+0.1)^2+9}$ into a digital IIR filter using bilinear transformation. The digital filter should have a resonant frequency of $Wr=\frac{\pi}{u}$? [8]

(b) Explain briefly the Filter Design Techniques. [8]

UNIT – V

Q.5 (a) Explain how DFT can be used as a linear transformation tool in Digital Signal Processing. [8]

(b) Explain various properties of the DFT in brief. [8]

OR

Q.5 Explain & find N-point DFT of following sequence $h(n)=\begin{cases}1/3 & \text{for } 0\le n\le 2\\ 0 & \text{else where}\end{cases}$ [16]

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7E7073

Roll No. ___________ Total No of Pages: 2

7E7073
B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electronic Instrumentation & Control Engineering
7EI4A Analytical & Environmental Instrumentation

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks Main: 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Define the term 'Fluorescence'. Explain the fluorescence spectrometers with suitable diagram. [8]

(b) Explain the 'Time of flight type mass spectrometer" with the neat sketch and mathematical equations. [8]

OR

Q.1 (a) "X – radiation provides powerful tools for analytical purposes" this statement is true or false, if true then explain How? [8]

(b) What is Beer – Lambert's Law? Explain the various terms involved in it. [8]

UNIT – II

Q.2 (a) Explain the working of Ultraviolet absorption gas analyzers. [8]

(b) How hydrocarbons are detected by Infrared gas analyzer? [8]

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OR

Q.2 (a) Differentiate the liquid phase and gas phase chemiluminescence detection. Explain the chemiluminescence based analyzers with neat sketch. [8]

(b) Explain the construction and working principle of paramagnetic oxygen analyzers. [8]

UNIT – III

Q.3 (a) What are the requirements of the detectors used in the gas chromatography? Explain "Electron Capture Detector' used in gas chromatography. [8]

(b) Explain the working principle, advantage & disadvantages of liquid chromatography. [8]

OR

Q.3 (a) Explain the utility and working of Flame ionization based detectors. [8]

(b) Explain the working principle, merits and demerits of thermal conductivity analyzers. [8]

UNIT – IV

Q.4 (a) What are air pollutants? How they are added in air? How solid suspended matters are measured in air? [8]

(b) How carbon monoxide (CO) and sulpher dioxide (SO_2) are measured in air? [8]

OR

Q.4 (a) Explain the importance of visible emission monitoring system. Explain its basic principle, merits and demerits. [8]

(b) Discuss about the hydrocarbon & ozone monitoring instruments with neat diagrams. [8]

UNIT – V

Q.5 Write short notes on the following:-

(a) Silica analyzers [8]

(b) Dissolved oxygen analyzers. [8]

OR

Q.5 Write short notes on the following:-

(a) Ammonia analyzers [8]

(b) pH meters [8]

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7E7074

Roll No. ____________ Total No of Pages: 3

7E7074

B. Tech. VII Sem. (Main/Back) Exam., Nov.-Dec.-2016
Electronic Instrumentation & Control Engineering
7EI5A Instrumentation in Industries

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main : 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

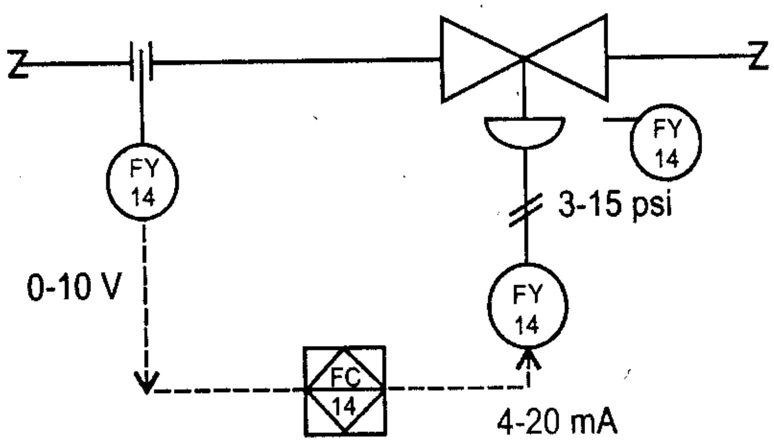
Q.1 (a) Draw and explain various instrument line symbols used in the process instrumentation drawings. [8]

(b) Explain the design goals of the instrumentation used in the plants. [8]

OR

Q.1 (a) Explain the standardized instrument symbols used in pipe and instrumentation diagrams. [8]

(b) Describe the instrument identification in the following P&ID diagram. [8]



UNIT – II

Q.2 (a) Explain the jacketed reactor temperature control with recirculation of cooling water. Show the effect of recirculation on sensitivity of reactor. [6+2=8]

(b) Draw and explain the pressure control scheme in continuous reactors. [8]

OR

Q.2 (a) What is meant by batch and continuous chemical reactors? Comment upon their conversion efficiency with reaction time. [5+3=8]

(b) What is cascade control? Explain the cascade control scheme for temperature with heating and cooling capability. [2+6=8]

UNIT – III

Q.3 (a) What is a heat exchanger? Draw the basic layout of a steam heater and explain degree of freedom in it. [3+5=8]

(b) Draw and explain the basic control strategy of condensate temperature control and condensing pressure control. [4+4=8]

OR

Q.3 (a) Draw and explain the control scheme of condensate throttling in heat exchangers. Mention its advantages. [6+2=8]

(b) Discuss the control schemes used in reboilers. [8]

UNIT – IV

Q.4 (a) Discuss the use of evaporators in plants. Explain single effect and multiple effect evaporators. [2+6=8]

(b) Differentiate between batch dryer and continuous fluid bed dryers with suitable diagrams. [8]

OR

Q.4 (a) Discuss the cascade control scheme used in evaporators. [8]

(b) Discuss the following control schemes of pumps - [4+4=8]

(i) ON-OFF pressure control

(ii) ON-OFF flow control

UNIT – V

Q.5 (a) Explain the control scheme used for feed water in power plants. [8]

(b) Explain the use of data loggers used in power plant instrumentation. [8]

OR

Q.5 Write short note on following -

(a) Interlocks used in power plants. [8]

(b) Steam temperature control in power plants. [8]

2a4

7E4054

Roll No. ____________ Total No of Pages: 2

7E4054
B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Electronic Instrumentation & Control Engineering
7EI3 (O) Computer Networks

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

Attempt any ***five questions****, selecting* ***one question*** *from* ***each unit****. All questions carry* ***equal*** *marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) What is the difference between Pure-death and Birth- death process? [8]

(b) State and prove Little's law and derive Little formulae. [8]

OR

Q.1 (a) Explain the mathematical model for m/m/m/m queue in details. [8]

(b) What is queuing system? In m/m/1 queuing, calculate average wait time of a packet in the queue. [8]

UNIT – II

Q.2 (a) Explain switching with its types and difference (any five). [8]

(b) Write short on: [4×2=8]

(i) Sliding window protocol

(ii) Selective repeat

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OR

Q.2 (a) What is framing? Define different framing schemes in the data link layer. [8]

(b) Write short note on: [4×2=8]

(i) OSI & TCP / IP reference models

(ii) Go back N protocol

UNIT – III

Q.3 (a) What is channel allocation? How Static and dynamic channel allocation has been achieved? [8]

(b) Define CSMA in details. [4]

(c) Explain working of 802.2 protocols. [4]

OR

Q.3 (a) What is FDDI? Discuss the strategy adopted in FDDI to serve the synchronous traffic requiring delay. [8]

(b) Write short note on:

(i) Token Ring [2]

(ii) Bridges [3]

(iii) Gateways [3]

UNIT – IV

Q.4 (a) Explain Dijkstra's shortest path algorithm using suitable example. [8]

(b) What are the differences between IPV6 and IPV4 protocols? [4]

(c) Explain congestion control algorithms for TCP / IP networks. [4]

OR

Q.4 (a) Explain TCP protocol architecture by drawing suitable header. [8]

(b) Write short note on:

(i) OSPF [4]

(ii) BGP [4]

UNIT – V

Q.5 (a) What is ATM? Explain recognition algorithm in ATM networks by drawing state diagram/flow chart. [8]

(b) Explain the characteristics of a connection oriented network. [8]

OR

Q.5 (a) Explain ATM protocol architecture. [8]

(b) What is ISDN system architecture? [4]

(c) What is difference between Frame Relay and ATM? [4]

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7E4055

Roll No. ___________ Total No of Pages: 3

7E4055

B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Biomedical Engineering
7BM6.3 Fiber Optic Instrumentation
EIC, BM

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions,** selecting **one question** from **each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain in details different types of fibers based on modes of propagation and index profile. Also draw index profile of various types of fibers with their applications. [10]

(b) A silica optical fiber with a core diameter large enough to be considered by ray theory analysis has a core refractive index of 1.50 and a cladding refractive index of 1.47. Find – (3×2=6)

(i) The critical angle at the core – cladding interface.

(ii) The numerical aperture of fiber.

(iii) The acceptance angle in air for the fiber.

OR

Q.1 (a) Compare the intrinsic absorption and extrinsic absorption in optical fiber. [8]

(b) A multimode graded index fiber exhibits total pulse broadening of 0.1MS over a distance of 15 km. Find –

(i) The maximum possible bandwidth of the link assuming no inter-symbol interference. [4]

(ii) The bandwidth length product for the fiber. [4]

UNIT – II

Q.2 (a) Draw and explain the structures of LED. [8]

(b) Explain in details different types of characteristics of LED. [8]

OR

Q.2 (a) Write short note on "fiber connectors". [8]

(b) Explain in detail expanded beam connectors with the help of diagram. [8]

UNIT – III

Q.3 (a) Describe the main factors which limit the speed of response of a photodiode. [8]

(b) The quantum efficiency of a particular silicon RAPD is 80% for the detection of radiation at a wavelength of 0.9μm. When the incident optical power is 0.5μW, the output current from the device (after avalanche gain) is 11μA. Determine the multiplication factor of the photodiode under these conditions. [8]

OR

Q.3 (a) Explain in detail the working principle of avalanche photodiodes with the help of diagram. [8]

(b) A photodiode has a quantum efficiency of 65% when photons of energy 1.5×10^{-19} J are incident upon it. [8]

(i) At what wavelength is the photodiode operating.

(ii) Calculate the incident optical power required to obtain a photocurrent of 2.5 μA when the photodiode is operating as described above.

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UNIT – IV

Q.4 (a) Briefly explain the measurement of total fiber attenuation of optical fibers. [8]

(b) Write short note on 'fiber dispersion measurements'. [8]

OR

Q.4 (a) Explain the fiber refractive index profile measurement in detail. [8]

(b) Explain with the help of diagram fiber numerical aperture measurements. [8]

UNIT – V

Q.5 (a) Explain the basic principle of laser in detail. [8]

(b) A GaAs injection laser has an optical cavity of length 250 μm and width 100 μm. At normal operating temperature the gain factor is 21×10^{-3} Acm^{-3} and the loss coefficient is 10 per cm. Determine the threshold current density and hence the threshold current for the device. It may be assumed that the cleaved mirrors are uncoated and that the current is restricted to the optical cavity. The refractive index of GaAs may be taken as 3.6. [8]

OR

Q.5 (a) Explain operation & applications of DFB Laser diode. [8]

(b) Compare the ratio of the threshold current densities at 20°C and 80°C for an AlGaAs injection laser with To = 160 K and the similar ratio for an InGaAsP device with To = 55 K. [8]

7E4056

Roll No. ___________ Total No of Pages: 2

7E4056

B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Electronics Instrumentation & Control Engg.
7EI5 Industrial Measurements

Time: 3 Hours **Maximum Marks: 80**

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any five **questions**, selecting **one question** from **each unit**. All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Explain Thermocouple with suitable diagram. [8]

(b) Explain Thermistor in detail & also explain its advantages and disadvantages. [8]

OR

Q.1 (a) Explain construction and working principle of optical pyrometer. [8]

(b) Compare Bimetallic thermometers with Resistance thermometer in detail. [8]

UNIT – II

Q.2 (a) Explain construction and working principle of strain gauge. [8]

(b) Write short notes on: - [8]

(i) Manometers

(ii) Bourdon tubes

OR

Q.2 (a) Explain Potentiometric Pressure Transducer with suitable diagram. [8]

(b) Define Piezo Electric effect and explain principle of capacitive pressure transducer. [8]

UNIT – III

Q.3 (a) Explain Rotameter flow meter in detail with suitable diagram. [8]

(b) Write short notes on: - [4×2=8]

(i) Orifice plate

(ii) Flow nozzles

OR

Q.3 (a) Explain ultrasonic flow meter in detail with suitable diagram. [8]

(b) Explain vortex flow meter in detail with suitable diagram. [8]

UNIT – IV

Q.4 (a) Explain capacitance level indicator with suitable diagram. [8]

(b) Explain construction and working of float type level measurement. [8]

OR

Q.4 (a) Explain hydrometers in density measurement. [8]

(b) Compare ultrasonic and radiation densitometer. [8]

UNIT – V

Q.5 (a) Explain foil type material of strain gauge. [8]

(b) Explain protective coating of strain gauge. [8]

OR

Q.5 (a) Explain application of Rosette gauge in detail. [8]

(b) Write short notes on: - [4×2=8]

(i) Bonding of strain gauge.

(ii) Calibration of strain gauge.

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7E4001

7E4001
B. Tech. VII Sem. (Back) Exam., Nov.-Dec.-2016
Biomedical Engineering
7BM1 Neural Networks and Fuzzy Logic Control
EIC, AI, BM

Time: 3 Hours **Maximum Marks: 80**
Min. Passing Marks Main : 26
Min. Passing Marks Back: 24

Instructions to Candidates:

*Attempt any **five questions**, selecting **one question from each unit.** All questions carry **equal** marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.*

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL 2. NIL

UNIT – I

Q.1 (a) Draw & Explain the working of Biological neural networks. [8]
(b) What are single & multilayer networks? [8]

OR

Q.1 (a) Define Perceptions. Explain the working logic of Perceptions & threshold logic devices. [8]
(b) Discuss artificial neuron model with suitable diagram. [8]

UNIT – II

Q.2 (a) Differentiate between supervised and unsupervised learning. Give example in support of your answer. [8]
(b) What are recent trends in learning algorithms? [8]

OR

Q.2 (a) Explain back propagation & feed forward methods applicable in learning algorithm. [8]

(b) Write short note on Hebbian learning with suitable example. [8]

UNIT – III

Q.3 (a) What do you mean by uncertainty in information? What are the rules of uncertainity & precision? [8]

(b) Discuss different fuzzy sets and membership. [8]

OR

Q.3 (a) What are features of membership function? Give its standard forms & boundaries. [10]

(b) What do you mean by membership value assignment? [6]

UNIT – IV

Q.4 (a) Discuss Defuzzification methods. Differentiate between centroid method and weighted average method. [8]

(b) What do you mean by mean max membership? [8]

OR

Q.4 Write short note -

(a) Aggregation of fuzzy rules. [8]

(b) Linguistic hedges. [8]

UNIT – V

Q.5 Explain special forms of FLC system models with suitable diagrams. [16]

OR

Q.5 Discuss the working of simple fuzzy logic controller. Give its industrial application. [16]
