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7E4048

Roll No. : _____ Total Printed Pages : 3

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B.Tech. (Sem. VII) (Main/Back) Examination, December-2012
Electronics & Comm.
7EC5 VLSI Design

Time : 3 Hours] [Maximum Marks : 80
[Min. Passing Marks : 24

Attempt any five questions. Selecting one question from each unit. All Questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. Nil

UNIT-I

1 (a) Compare bipolar junction transistor with field effect transistor. What is basic MOS transistor ? What are different kinds of MOS transistor ? Explain the structure and operation of a basic MOS transistor. 3+2+2+3

(b) How an nMOS transistor is fabricated ? Explain the basic steps of nMOS fabrication in detail. 6

OR

1 (a) What do you understand by enhancement mode transistor action and depletion mode transistor action ? What is the difference between them. 4+4+2

(b) What are different techniques of CMOS fabrication ? Explain one of them in detail. 6

UNIT-II

2 (a) Derive the I_{DS} - V_{DS} relationship for enhancement type MOSFET :

(i) For Ohmic Region

(ii) For Saturation Regior

8

(b) Design a resistive-load inverter w ch R = 1 KΩ, such that at V_{OL} = 0.6V. The enhancement type nMOS driver transistor has the following parameters V_{DD} = 5V, V_T = 1V, $\mu_n Cox = 22\mu\ A/V^2$.

(a) Determine the required aspect ratio W / L.

(b) Determine noise margins NM_L and NM_H.

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OR

2 (a) How the V-I characteristic modify with channel length modulation effect ? Show it on V-I characteristic and in V-I relation ? What do you understand by transistor trans conductance ?

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(b) Write short notes on :

(i) Noise Margins

(ii) Pull-up to Pull-down ratio for an nMOS inverter.

4+4

UNIT-III

3 (a) What is CMOS transmission gate ? Draw half-adder and half-subtracter circuit using it.

2+3+3

(b) Define Delay-Time. Derive the expression for τ_{PHL} for CMOS inverter by using state equation method.

2+6

OR

3 (a) Design the following CMOS logic :

(i) Two bit magnitude comparator for the case A < B

(ii) Equality Detector circuit

4+4

(b) Briefly discuss analytical delay model based on switching characteristic of CMOS in water also define delay times using average current method.

4+4

UNIT-IV

4 (a) What do you mean by stick diagram ? Draw the stick diagram for :
(i) CMOS inverter
(ii) Two input NAND gate

2+3+3

(b) Draw the physical layout for $F = \overline{wx + yz}$.

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OR

4 (a) Write short note on layout design rules. Draw the layout diagram for two input NAND gate and two input NOR gate.

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(b) What is euler path ? What is the use of it ? Find the euler path for F = AB + CD + AC.

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UNIT-V

5 (a) Distinguish between :
(i) Signal and Variable
(ii) Concurrent and Sequential assignment
(iii) Behavioral and Structural Modelling.

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(b) Write VHDL code on any **two** :
(i) D - flip flop
(ii) T - flip flop
(iii) J - K flip flop

8

OR

5 (a) Differentiate between all modeling styles of an architecture body.

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(b) Explain the following statements of VHDL with example :
(i) Process Statement
(ii) Wait Statement
(iii) Assertion Statement
(iv) Block Statement.

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