7E4048

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B. Tech. VII Semester (Main/Back) Examination, Nov-Dec - 2011

Electronics & Communication Engineering

7EC5 VLSI Design

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 24

Instructions to Candidates:

*Attempt any **five questions** selecting **one question** from **each unit**. All questions carry **equal marks**. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Unit - I

1. a) Draw the MOS transistor circuit modal. Give the justification for all capacitance. Compare the different capacitance. Explain in detail for overloop capacitance. **(12)**

   b) Write and explain equation for V-I relationship of MOS transistor. **(4)**

OR

1. a) Draw and explain various step involved in n-well CMOS fabrication. **(8)**

   b) Write comparative discussion of 'Twin-tub CMOS fabrication' and 'Silicon - on - insulator' fabrication process. **(8)**

Unit - II

2. a) What are various second order effect? Explain how V-I characteristics modify with channel length modulation effect? Show it on V-I characteristics and in V-I relation. **(10)**

   b) What is body effect? Write equations related to body effect threshold voltage. **(6)**

OR

2. a) Calculate the V_{TO} NMOS, Given that $V_{SB}=0$, $ni=1.45\times10^{10}$, $N_A=10^{16}$ $N_D(gate)=2\times10^{20}$. Gate electrode is polysilicon $tox=500^{o}A$. (Oxide thickness $Qox=4\times10^{10}$), here Cox static charge. **(10)**

b) Explain the influence of $\frac{\beta_n}{\beta_p}$ ratio on CMOS inverter DC transfer characteristic. **(6)**

Unit - III

3. a) Why does NMOS transistor produces strong '0' and weak '1' while PMOS transistor produces strong '1' and weak'0'? **(8)**

b) Explain working of transmission gate. or pass transistor. What are advantages and disadvantages of transmission gate. **(8)**

OR

3. a) Design the following CMOS logic

i) $Y=\overline{A+BC+DE}$

ii) $Y=AB+\overline{AB}$ **(8)**

b) Explain and derive the expression for dynamic power dissipation of CMOS circuit. **(8)**

Unit - IV

4. a) Draw the stick diagram for

i) CMOS EX-OR Gate

ii) 2:1 MUX **(10)**

b) Explain different types of layout design rules. **(6)**

OR

4. a) Draw the physical layout for $X=\overline{ab+CD}$ **(8)**

b) Design layout for an n-diff wire connected to p-diff wire. **(8)**

Unit - V

5. a) Write VHDL code for half adder by following modelling style.

   i) Data flow

   ii) Behavioral

   iii) Structural **(12)**

   b) Write VHDL code for J-K flip-flop. **(4)**

OR

5. a) Write VHDL code for 3-bit counter. **(4)**

   b) Write short notes on any **Three** of following. With references to the VHDL.

   i) Process statement

   ii) Test-bench

   iii) Types of delay

   iv) Advantages and limitation of VHDL. **(12)**