8E4015

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B. Tech. (Sem. VIII) (Back) Examination, April/May-2012
Computer Science
8CS2(O) CAD FOR VLSI Design

Time : 3 Hours] [Total Marks : 80
[Min. Passing Marks : 24

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. (Schematic diagrams must be shown wherever necessary.) Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. Nil 2. Nil

UNIT - I

1 (a) **Explain the process of Digital System Design with the help of flow diagram.** 8

(b) **What do you understand by FPGA design ? Explain the FPGA design flow with the help of flow chart.** 8

OR

2 (a) **Explain the significance of Productivity Gap in terms of time to the Market and Design Complexity.** 8

(b) **Describe the following terms in connection with ASIC Design process.**
(i) Logic synthesis and system partitioning
(ii) Prelayout simulation
(iii) Floor planning and Placement
(iv) Routing and Extraction. 8

[Contd...

UNIT - II

3 (a) How VHDL differs from other software programming languages in terms of advantages ? Explain the basic requirement features of VHDL. 2+6

(b) Describe and write syntax for following in VHDL.
(i) Entity and Architecture.
(ii) Package
(iii) Configuration and Binding Approach. 8

OR

4 (a) Explain the Level of Abstraction in VHDL with suitable examples. 8

(b) Explain the constraint to characterize the Hardware Description Languages. What do you mean by Top-Down Approach in VHDL ? 8

UNIT - III

5 (a) Describe the following terms in VHDL with suitable example.
(i) Transport Delay and Inertial Delay
(ii) Multiple Drivers 8

(b) Describe the various types of operators used in VHDL. 8

OR

6 (a) Draw the waveform for below mentioned code.

```
Architecture sequential of discarding-old is
SIGNAL x : bit := 'Z' ;
BEGIN
    PROCESS
        BEGIN
        X < = '1' After 5 ns;
        X <= Transport '0' after 3 ns;
    Wait;
end PROCESS;
end sequential;
```

8

(b) Write the VHDL code for half adder circuit using all three types of modelling styles. 8

UNIT - IV

7 (a) Write short notes on the following :

(i) Overloading concept in VHDL.

(ii) Difference in predefined attributes and user defined attributes. 8

(b) Explain VHDL subprogram parameters. 8

OR

8 Explain the following with suitable examples.

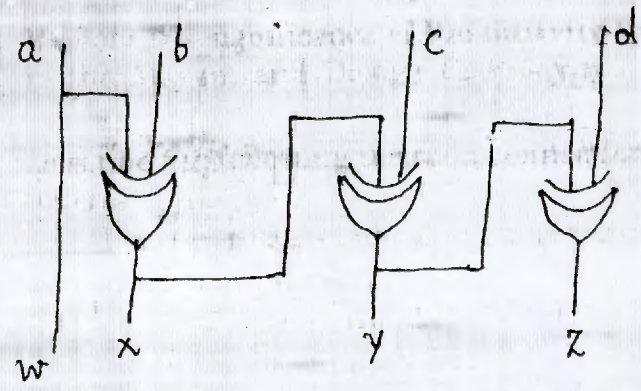
(a) Bi-Directional component modeling.

(b) Multi-mode component modelling. 8+8

UNIT - V

9 (a) Write the VHDL code for 8 bit shift register with positive-edge clock and serial in serial out. 8

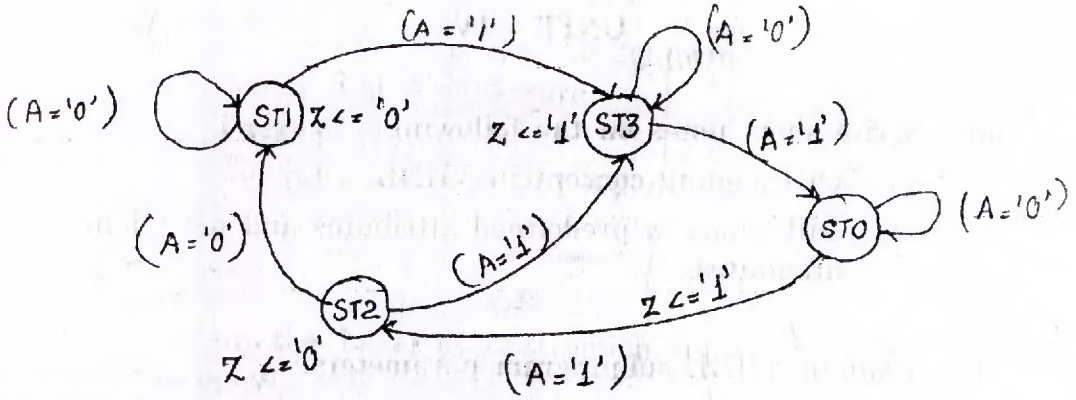
(b) Write the VHDL code for Gray to Binary Converter Circuit Diagram is given below. 8



OR

10 (a) What is the difference between Mealy and Moore Machine. 6

(b) Write the VHDL code for following Moore FSM. State diagram is given below.



Assuming 'A' and clk as input signal, Z as output signal ST0, ST1, ST2, ST3 are state types. 10

CS Book
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