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7E4093

Roll No. : _____ Total Printed Pages : 3

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B. Tech (Sem. VII) (Re-Back) Examination, December-201 .
Computer Engg.
7CS3 Logic Synthesis

Time : 3 Hours] [Maximum Marks : 80
[Min. Passing Marks : 24

Attempt overall Five questions selecting one question from each unit. All questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing may suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly).

Use of following supporting material is permitted during examination.
(Mentioned in form No. 205)

1. NIL 2. NIL

UNIT - I

1 (a) What do you mean by ASIC's ? 2

(b) Explain VLSI and Moore's law. 6

(c) Explain steps for designing and integrated circuit. 8

OR

1 (a) Make Binary Decision Diagram and convert it into Reduce order Binary Decision Diagram. 6
$f = (a + b) \cdot C$

(b) Explain design styles of micro electronics chips. 6

(c) Explain following : 4
(i) Clique No
(ii) Cromatic No
(iii) Directed and indirected graph
(iv) Simulation and verification.

UNIT - II

3 (a) What is structural representation using modules pins and nets ? Give one example using hypergraph and biparate graph representation.

(b) Explain 'Partial binding' with example. 8

OR

4 (a) Explain temporal domain scheduling and give one example. 8

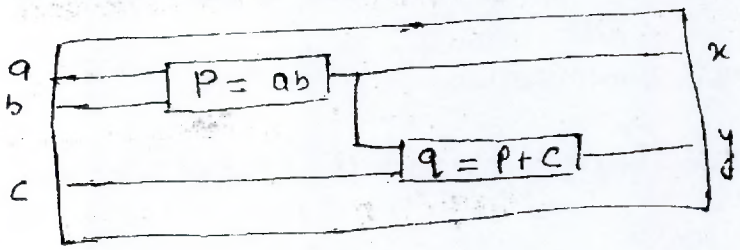
(b) Given the following net list, show two other possible representation.

$m_1 = n_1, n_2$

$m_2 = n_1, n_2, n_3$

$m_3 = n_2, n_3$ 4

(c) Draw a logic graph for the given logic network.



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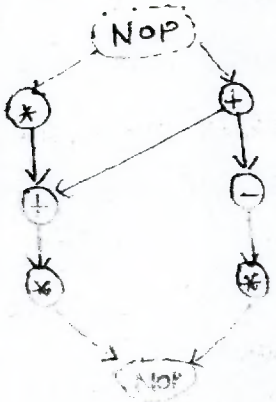
UNIT - III

5 Consider the graph as given below. Assume the execution delay of multiplier and of the ALU are 3 cycles and 2 cycles respectively schedule the graph using

(a) ASAP Algo

(b) ALAP Algo when the latency bound $\pi = 12$ cycles

(c) Determine the mobility of the operation.



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OR

6 (a) Schedule the sequencing graph (as given in Q No. 5) using minimum resource latency constrained when multiplier take 2 cycles and ALU take 1 cycle. Assume the latency bound $\pi = 5$ cycles. And determine minimum resource required for scheduling. **10**

(b) Explain well posed and illposed timing constraint with example. **6**

UNIT - IV

7 (a) Explain Heuristic logic minimization. **8**

(b) Explain following with example.
(i) Sharp (#) operation
(ii) Disjoint sharp (Ⓐ) Operation. **8**

OR

8 (a) Explain Exact logic minimization. **8**

(b) Explain programable Logic Array with the help of diagram. **8**

UNIT - V

9 (a) Explain state minimization for completely specified finite state machine with example. **8**

(b) Explain state minimization for incompletely specified finite state machine with example. **8**

OR

10 (a) Explain the sequential circuit optimization using network model. **10**

(b) Explain the testability consideration for synchronous circuits. **6**