7E4093

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7E4093

B. Tech. VII Semester (Back) Examination, Nov-Dec-2011

Computer Science

7CS3 Logic Synthesis

Time : 3 Hours **Maximum Marks : 80**

Min. Passing Marks : 24

Instructions to Candidates:

*Attempt any **five questions** selecting **one question** from **each unit.** All questions carry **equal marks.** Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.*

Unit - I

1. a) What are the different phases in creating microelectronic chips? **(6)**

   b) Which four numerical properties characterize a graph? Give suitable examples. **(1.5×4=6)**

   c) Draw an OBDD for a three-input OR gate and then draw its ROBDD. **(2+2=4)**

OR

1. a) What are the different styles of microelectronic design? Compare them. **(6)**

   b) Consider the function $f = (a + b)\,(b + c)\,(c + a)$.

      i) Find out Boolean derivative with respect to variable a.

      ii) Find out Boolean consensus with respect to variable b. **(2×2=4)**

   c) Give one algorithm each for the following

      i) Vertex cover problem

      ii) Single source shortest path problem. **(3×2=6)**

Unit - II

2. a) Differentiate between Hardware description languages and Software programming languages. **(3)**

   b) How can circuit models be classified based on level of abstraction and based on view? **(3×2=6)**

c) What are scheduling and binding in architectural synthesis? (2×2=4)

d) How is area and performance estimation done in resource dominated circuits? (3)

OR

2. a) How are circuits modeled using the sequencing graphs? (6)

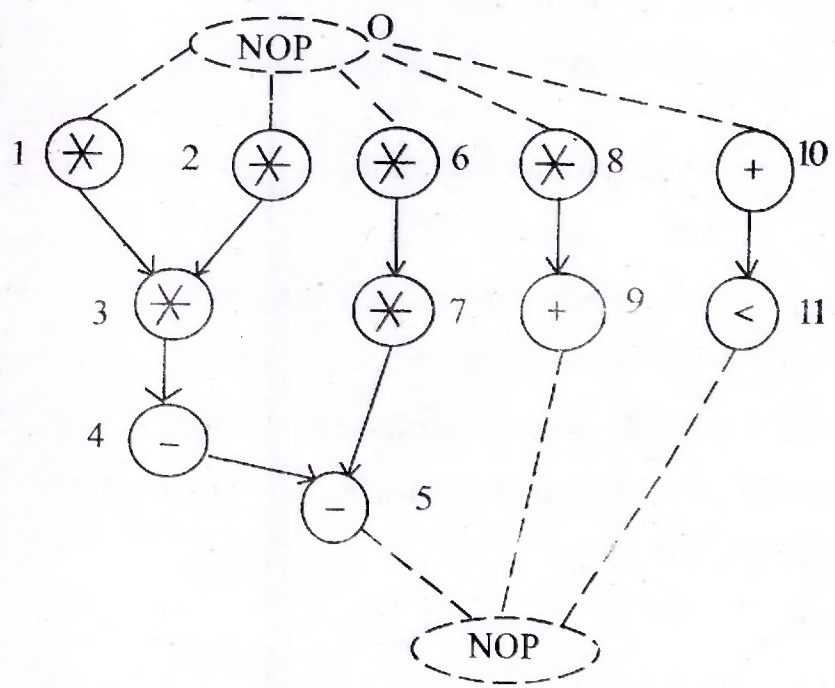
b) Differentiate between software compilation and hardware compilation (3)

c) What are hierarchical models? (3)

d) What do you understand by resources and constraints in architectural synthesis? (4)

Unit - III

3. For following sequencing graph obtain integer linear programming constraints, assuming ALU takes one unit of time and multiplier takes two units of time. Only two instances of each type of resources are available, $a=\{2,2\}$. Upper bound on latency is $\bar{\lambda}=4$ (16)

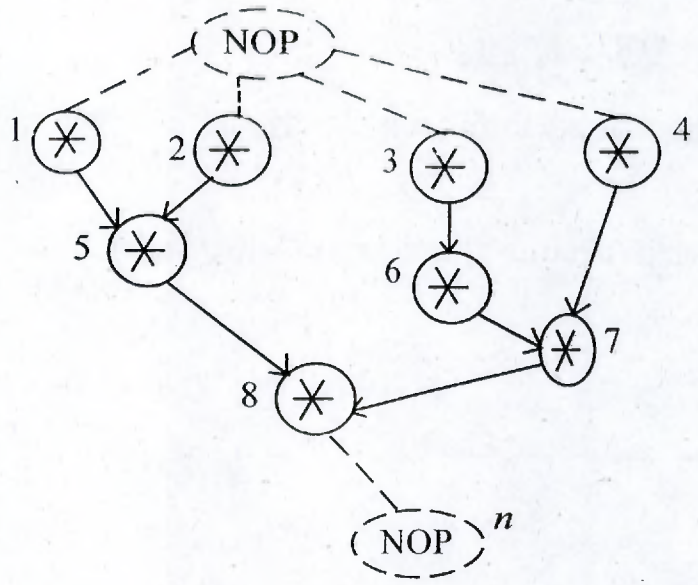


OR

a) Give the List scheduling algorithm for minimum resource latency constrained scheduling (6)

b) Giving one example explain constraint graph. What is welt posed and feasible constraint graph? **(6)**

c) For the given sequencing graph find number of resources required to schedule it in 4 time steps, with unit execution delay for every operation. **(4)**



Unit - IV

4. a) Write short notes on :

i) Exact logic minimization

ii) Positional cube notations. **(2×7=14)**

b) When can you call a circuit fully testable? **(2)**

OR

4. a) What is two level logic optimization? **(4)**

b) Define and illustrate with examples

i) implicant

ii) redundant cover **(2×3=6)**

c) Write a short note on Heuristic Logic minimization? **(6)**

Unit - V

5. Describe the following :-

   i) Retiming

   ii) Constrained state encoding (8×2=16)

OR

5. a) Differentiate between state minimization for completely and incompletely specified state machines. **(8)**

   b) Explain the modeling of sequential circuits by synchronous logic networks. **(8)**
