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5E3253

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# 5E3253
# B.Tech. V Sem.(Main/Back) Exam Dec. 2012
## Computer Science
## 5CS2 Digital Logic Design

**Time : 3 Hours** **Maximum Marks : 80**
**Min. Passing Marks : 24**

*Instructions to Candidates:*

*Attemept any **five question** selecting **one question** from **each unit** .All Question carry equal marks. Schematic diagrams must be shown wherever necessary . Any data you feel missing suitably be assumed and stated clearly. Units of quantities used / calculated must be stated clearly.*

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. **NIL** 2. **Nil**

## UNIT - I

Q.1 (a) What are the Data Type in VHDL? Explain with Example. 8

(b) What are the Basic Modeling Constructs in VHDL? 8

## OR

Q.1 (a) Explain the Concept of Look Ahead Carry Adder. 8

(b) Write Code for Ripple Carry Adder. 8

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## UNIT - II

Q.2 (a) Explain Packages in VHDL. 4

(b) Explain use Clauses in VHDL. 4

(c) Explain Simulation in VHDL. 4

(d) Explain Synthesis in VHDL. 4

**OR**

Q.2 (a) Explain Components in VHDL. 4

(b) Explain Configuration in VHDL. 4

(c) Explain Generate statement in VHDL. 4

(d) Explain Concurrent statement in VHDL. 4

## UNIT - III

Q.3. (a) Explain Moore Machine and describe the clock skew. 8

(b) Explain Concept and working of ROM and PLA. 8

**OR**

Q.3. (a) Explain Melay Machine and describe the clock skew. 8

(b) Explain Concept and working of FPGA and PLD. 8

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# UNIT - IV

Q.4 (a) What is Hazards? Define Logic Hazards and Function Hazards. 8

(b) Describe Dynamic Hazard with Diagram. 8

## OR

Q.4 (a) What is Asynchronous circuit? Write design Procedure for Asynchronous circuit. 8

(b) What is Compatibility and state reduction procedure? 8

# UNIT - V

Q.5 (a) What is design process of FPGA? 8

(b) Write short note on SRAM or Flash Memory. 8

## OR

Q.5 (a) Write short note on FPGA. 8

(b) Write short note on logic synthesis. 8

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