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5E3160

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# 5E3160
## B. Tech. V Sem.(Re-Back) Exam. -Dec. 2012
## Computer Science
## 5CP/CS2 Computer Architecture
## Common With 5IT2

**Time : 3 Hours** **Maximum Marks : 80**

**Min. Passing Marks : 24**

*Instructions to Candidates:*

*Attempt any **five questions.*** Selecting **one question** from **each unit.** All Question carry **equal** marks. Schematic diagram must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.

1. **Nil** 2. **Nil**

## UNIT - I

Q.1(a). Represent the following conditional control statements by two register transfer statements with control functions:

If (P=1) than (R1 ← R2) else if (Q=1) then (R1 ← R3) (8)

Q.1(b) A digital computer has common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. (8)

(i) How many selection inputs are there in each multiplexer?

(ii) What size of multiplexer is needed?

(iii) How many multiplexers are there in the bus?

**OR**

1. (a) Design Arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with input carry $C_{in}$. Draw a logic diagram for first two stages. (8)

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| S | $C_{in.} = 0$ | | $C_{in.} = 1$ | |
|---|---|---|---|---|
| 0 | D=A+B | Addition | D = A+1 | Increment |
| 1 | D= A-1 | Decrement | D = A+B'+1 | Subtraction |

Q.1 (b) Design a 4-bit combinational circuit decrementor using four full adder circuits. (8)

## UNIT –II

Q.2 (a) Write all possible addressing modes. Explain each by taking appropriate example. (8)

Q.2 (b) What is pipelining? What is the maximum speed up that can be Attained ? Construct an instruction pipeline. Is it possible to attained maximum speed up in an instruction pipeline? (8)

**OR**

Q.2 Write a program to evaluate the arithmetic statement: (16)

$$X = \frac{A+B*C-D}{E+F*G}$$

(i) Using general register computer with three address instruction.

(ii) Using general register computer with two address instruction.

(iii) Using accumulator type computer with one address instruction.

(iv) Using stack organized computer with zero address instruction.

## UNIT –III

Q.3 Draw Flowchart of multiplying two binary numbers using Booths algorithm. (1

Perform (-15)*(+13) using Booths algorithm.

**OR**

Q.3 Explain the algorithm of addition and subtraction for singed magnitude data. Also give hardware implementation of expl (

algorithm [1

# UNIT -IV

Q.4 (a) Explain the difference between hardwired control and microprogammed control . Is it possible to have hardwired control associated with control memory.? (8)

**OR**

Q.4 (b) Explain basic structure of micro programmed control unit. (8)

Q.4 Give schematic diagram of micro program sequencer. Also describe horizontal and vertical microcode format used in control unit design. (16)

# UNIT - V

Q.5 (a) A block set associate cache consist of total 64 block divided into four blocks per set. The main memory contains 4096 blocks each consisting of 128 words. (8)

a) How many bit are there in main memory address.
b) How many bits are there in Tag, SET and Word field?

Q.5 (b) Differentiate between strobe based and handshake based communication. (8)

**OR**

Q.5 (i) How many 128*8 RAM chips are needed to memory capacity of 2048 bytes?

(ii) How many lines of address must be used to access 2048 bytes of memory ? How many of these lines will be common to all chips.

(iii) How many line must be decoded for chip select? Specify the size of decoders. Show the memory connection of these chips with CPU. (16)

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