

ES102

Roll No. \_\_\_\_\_

Total No of Pages: 2

### 5E5102

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 Computer Engineering 5CS2A Digital Logic Design

Time: 3 Hours

**Maximum Marks: 80** 

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

### Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. <u>NIL</u>

2. NIL

### <u>UNIT – I</u>

Q.1 Explain Hardware Description Languages and their use in digital logic design in detail along with their application areas. [16]

#### OR

Q.1 (a) Describe scalar date types & operations in VHDL.

[8]

(b) Explain scalar date types & operations in VHDL.

[8]

### <u>UNIT – II</u>

Q.2 Write Technical notes on following -

(a) Packages & Use Clauses in VHDL.

[8]

(b) Components & configurations in VHDL.

[8]

[5E5102]

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[6600]

	$\underline{\mathbf{OR}}$	
Q.:	2 What are concurrent statements in VHDL. Also explain use of VH	IDL in simulation
	and synthesis of digital circuits with example.	[16]
	<u>UNIT – III</u>	[**]
Q.:	3 (a) Write and explain design steps for synchronous sequential circu	its. [8]
	(b) Write short note on programmable logic devices in detail.	[8]
	<u>OR</u>	[∨]
Q.3	Explain the process of converting ASM charts to hardware a	and also explain
	Algorithmic state charts in detail along with concept of set-up time ar	nd hold time. [16]
	<u>UNIT – IV</u>	
Q.4	Explain in detail dynamic hazards, function hazards, and esse	ntial hazards in
	combinational networks.	[16]
	<u>OR</u>	[10]
Q.4	(a) What are stable and unstable states. Explain the concept of rac	ces and race-free
	assignments in detail.	[10]
	(b) Write short note on compatibility and state reduction procedure.	[6]
	<u>UNIT – V</u>	[o <sub>j</sub>
2.5	Explain following incorporate with field programmable gate arrays.	[8×2=16]
	(a) Logic elements & programmability.	[0/2-10]
	(b) Interconnect structures & programmability.	
	<u>OR</u>	
).5	Write short notes on -	[8×2=16]
	(a) Extended Logic elements in FPGA.	[0]
	(b) Flash Memory & anti-fuse configuration in FPGA.	

**SES103** 

Roll No.

Total No of Pages: 3

### 5E5103

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 Computer Engineering 5CS3A Telecommunication Fundamentals

Time: 3 Hours

**Maximum Marks: 80** 

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units bf quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. NIL

### UNIT - I

- Q.1 (a) Draw the following reference models used in computer communication -
  - (i) OSI / ISO Model
  - (ii) TCP/ IP Model
  - (b) Explain the stop and wait ARQ Protocol and also discuss the Piggy backing method. [8]

### <u>OR</u>

Q.1 (a) In a Microwave communication link, two identical antennas operating at 10 GHz are used with power gain of 40db. If the transmitter power is 1 W, find the received power if the range of the link is 30km. [8]

[5E5103]

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[7600]

[8]

	(0)	what do you understand by synchronization problem? How to solve it? Explain
		with suitable example. [8]
		<u>UNIT – II</u>
Q.2	(a)	Show that slotted ALOHA has a maximum throughput of twice the pure ALOHA
		maximum throughput.
	(b)	Explain the frame structure of point to point protocol. What is difference between
		HDLC and PPP? [8]
		<u>OR</u>
Q.2	(a)	A 1 km, 10MbPS CSMA/CD LAN has a propagation speed of 200m/ μ sec. Data
		frames are 256 bits long, including 32 bits of header. Check sum and other
		overhead for the receiver to capture the channel to send a 32 bit
		acknowledgement frame. What is effective data rate excluding overhead,
		occurring there are up a 11' ' 0
	(b)	Explain the frame structure of point to point protocol. What is difference between
		HDLC and PPP? [8]
		<u>UNIT – III</u>
<b>Q</b> .3	(a)	What is looping problem in switching? Explain spanning. Explain spanning Tree
		protocol in detail. [10]
	(b)	What is the difference between a forwarding port and a blocking port? [6]
		<u>OR</u>
<b>Q</b> .3	(a)	What is Hidden Node and Exposed Node problem? Explain with example. [8]
	(b)	What is the function of L2CAP layer in Bluetooth? [4]
	(c)	Explain Piconet and Scatternet in Bluetooth. [4]
		<u>UNIT – IV</u>
Q.4	(a)	Assume that the velocity of propagation on a TDM bus is 0.8 c (c = Speed of
		light), its length is 10M, and the data rate is 500 MbPS. How many bits should be
		transmitted in a time slot to achieve a bus utilization of 99%? [8]

(b) Explain TDMA superframe structure. Are collisions possible i	in TDMA and
	[8]
FDMA? Justify.	
<u>OR</u>	ſQ1
Q.4 (a) Describe ADSL. Also discuss the two systems used in ADSL.	[8]
Consider a PCM system in which 24 signals are to be time divisi	on multiplexed.
(b) Consider a PCM system in which 24 signals are to Each signal has a 3 kHz bandwidth. The sampling rate is 33.3 per	cent higher than
Each signal has a 5 kHz ballowidth. The ballowidth and part and for each sample.	
the theoretical maximum and 8 bits are used for each sample.	
(i) Determine the required bit rate.	[4]
	[4]
(ii) Find the minimum required transmission bandwidth.	
<u>UNIT – V</u>	hamad
Q.5 (a) What are the various spread spectrum techniques? Explain fr	equency nopped
spread spectrum technique.	fol
and reverse CDMA channel!	[8]
<u>OR</u>	[4×2=8]
Q.5 (a) Define following (Any two):	[4/12-10]
,	
(i) M- sequence	
(ii) Hand off	
(iii) IMT - 2000	,
(b) What is Walsh Code Synchronization? Explain.	[8]

Roll No. Total No of Pages: 4 5E5104 B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 **Computer Science & Engineering 5CS4A Database Management System** Common with CS, IT Time: 3 Hours **Maximum Marks: 80** Min. Passing Marks Main: 26 Min. Passing Marks Back: 24 Instructions to Candidates: Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly. Use of following supporting material is permitted during examination. (Mentioned in form No. 205) 1. <u>NIL</u> 2. NIL UNIT – I Q.1 (a) What do you means by DBMS? Explain the advantages of Database Management system over file management system. [10] (b) What is difference between logical data independence and physical data independence. [6] OR Draw the diagram of system structure of DBMS. Write down the main function Q.1 (a) of each component. Why query processor component of database is important? Briefly discuss about all components of query processor. [5] Differentiate between DDL & DML. [3]

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[7200]

[5E5104]

### UNIT – II

		<u>UNII - II</u>	
Q.2	(a)	What is the role of ER model in database design? Draw an ER diagra	m for
~		library management system and convert ER-Diagram into tables. [2+6+	-4=12]
	(b)	What do you means by constraints? Explain different types of constraint	s with
		examples.	[4]
	•	<u>OR</u>	
Q.2	(a)	Explain the following with the help of suitable Examples:	
		(i) Participation constraints	
		(ii) Aggregation	
		(iii) Multi - valued Attributes	
		(iv) Key constraints	2×4=8]
	(b)	Design an E-R Diagram to show that participation of weak entity set as	owner
		entity set in identifying relationship with another weak entity sets ar	nd find
		primary key of all entity sets.	[4]
	(c)	Explain concept of specialization and generalization in E - R model.	[4]
		<u>UNIT – III</u>	
Q.3	(a)	Explain following operations in relational algebra with suitable examples:	
		(i) Rename	
		(ii) Natural Join	
		(iii) Division	
		(iv) Grouping [3	3×4=12]
	(b)	Differentiate relation algebra and relational Calculas.	[4]
	.* •	<u>OR</u>	
Q.3	3 (a)	Consider following schemas: [4	4×3=12]
		Passengers (Name, Address, Age)	
		Reservations (Name, FlightNum, seat)	

Flights (<u>FlightNum</u>, DepartCity, DestinationCity, MinutesLate, DepartureTime, ArrivalTime)

- (i) Get the names of passengers who had a reservation on a flight that was more than 30 minutes late.
- (ii) Get the names of passengers who had reservations on all flights that were more than 60 minutes late.
- (iii) Get the names of pairs of passengers, who are of the same age.
- (b) Discuss various types of inner join operation.

[4]

### UNIT - IV

Q.4 Consider the employee database given below:

 $[4 \times 4 = 16]$ 

Employee (emp\_name, street, city)

Works (emp\_name, company\_name, salary)

Company (company\_name, city)

Manages (emp\_name, manager\_name)

Give an expression in SQL for each of the following queries:

- (i) Modify the database so that Jones now lives in New town.
- (ii) Give all managers of First Bank Corporation a 10 percent raise.
- (iii) Give all managers of First Bank Corporation a 10 percent raise unless the salary becomes greater than \$100,000; in such cases, give only a 3 percent raise.
- (iv) Find the names of all employees in this database who live in the same city as the company for which they work.

#### <u>OR</u>

- Q.4 (a) What is Triggers? How do we create triggers on a database? Show some syntax.
  - (b) Explain Embedded SQL and Dynamic SQL.

[8]

# <u>UNIT – V</u>

Q.5	(a)	Discuss the purpose of BCNF and describes how BCNF is different f	from 3NF
		Provide an example to illustrate the answer.	[12]
	<b>(b)</b>	What is Decomposition? Explain Lossy and Lossless join decompositio  OR	n. [4]
Q.5		are given a schema s = {A,B,C,D,E}. The F of functional dependencies is	s <b>{A→ B</b> ,
	BC	$\rightarrow$ E, ED $\rightarrow$ A}.	
	(a)	is S in BCNF? Why?	[3]
	(b)	is S in 3NF? Why?	
•	(c)	Find canonical cover F <sub>C</sub> of F	. [3]
	(d)		[5]
٥	(ω)	List all candidate keys for S	[5]

SE5105

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### 5E5105

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 Computer Science & Engineering 5CS5A Operating Systems Common with CS, IT

Time: 3 Hours

**Maximum Marks: 80** 

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

### Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. (Mentioned in form No. 205)

1. NIL

2. <u>NIL</u>

### UNIT - I

- Q.1 (a) What are the different services provided by the operating system? Explain all of them in detail?
  - (b) What are the five major activities of an operating system with regard to file management? [8]

### <u>OR</u>

- Q.1 (a) What are the two models of interprocess communication? What are the strengths & weakness of the two approaches? [8]
  - (b) What are the difference between user level threads & kernel Level threads, under what circumstances is one type better than the other? [8]

[5E5105]

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[6680]

### <u>UNIT – II</u>

- Q.2 (a) In connection with interprocess communication explain the following: [8]
  - (i) Race Condition
  - (ii) Critical Condition
  - (iii) Sleep & Wake up
  - (iv) Sleeping Barber's Problem
  - (b) Define scheduling criteria? Explain Quencing diagram for the CPU scheduling in detail?

#### <u>OR</u>

- Q.2 (a) Describe the difference between short term, medium term, & long term scheduling?
  - (b) Consider the following set of processes, with the arrival times and the CPU burst times given in milliseconds.

    [8]

PROCESS	ARRIVAL TIME	BURST TIME
PI	0	5
, P2	1	3
Р3	2	3
P4	4	1

What is the average turn around time for these processes with the preemptive shortest remaining process time first algorithm?

## <u>UNIT - III</u>

- Q.3 (a) Explain Banker's Algorithm for deadlock avoidance with an example?
- [5E5105] Page 2 of 4

[8]

(b) Apply deadlock detection algorithm to the following data & show the results: [8] Available = (2, 1, 0, 0)

Request = 
$$\begin{pmatrix} 2 & 0 & 0 & 1 \\ 1 & 0 & 1 & 0 \end{pmatrix}$$

### <u>OR</u>

Q.3 (a) With the help of neat diagram Explain Memory hierarchy in detail? [8]

(b) Explain the difference between Paging & Segmentation? [8]

### <u>UNIT – IV</u>

Q.4 (a) Write Short note on Page Replacement Algorithms in Detail? [8]

(b) Let 620 frames are split between two processes, one of 100 pages & one of 1270 pages. Find the number of frames allocated for each process if proportional allocation method is used?
[8]

#### <u>OR</u>

Q.4 (a) What is Belady's Anamoly? In which algorithm does it occur? [8]

(b) Consider the following segment table. [8]

SEGMENT	BASE	LENGTH
0	219	600
1	2300	14
2	90	100
3	1327	580
4	1952	96

Calculate the physical address for the following logical addresses?

### <u>UNIT - V</u>

Q.5 (a) Define file system? Explain file operations in detail?

[8]

(b) Explain the classification of Allocation Methods?

[8]

#### <u>OR</u>

- Q.5 (a) Explain the Concept of spooling with all its types and its advantages & disadvantages? [8]
  - (b) Suppose the head of moving head disk is currently servicing a request at track 60.

    If the queue of request is kept in FIFO order, what is the total head movement to satisfy these requests for the following disk scheduling algorithm:

    [8]
    - (i) FCFS
    - (ii) SSFT

REQUEST SEQUENCE	TRACK NUMBER
1	56
2	170
3	35
4	120
5	. 10
6	140

Total No of Pages: 4 Roll No. 5E5106 B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 Computer Science & Engineering **5CS6.1A Advance Data Structure** Common with CS, IT **Maximum Marks: 80** Time: 3 Hours Min. Passing Marks Main: 26 Min. Passing Marks Back: 24 Instructions to Candidates: Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly. Use of following supporting material is permitted during examination. (Mentioned in form No. 205) 2. NIL\_\_ 1. <u>NIL</u> UNIT - I Given an element x in an n-node order-statistic tree and a natural number i, how Q.1 (a) can the ith successor of x in the linear order of the tree be determined in O(log n) [8] time. (b) Describe an efficient algorithm that, given an interval i, returns an interval overlapping i that has the maximum low endpoint, or nil [T] if no such interval [8] exists. OR Q.1 (a) Does deleting a leaf node from a red-black tree then reinserting the same key always result in the original tree? Prove it does or given a counter example where [8] it does not. Write a method in C to erase a pair in the dictionary with the Key in a skip list

representation. What is the complexity of this method?

[5E5106]

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[8]

[5700]

### <u>UNIT – II</u>

- Q.2 (a) Explain Amortized Cost of Incrementing Binary Integers and potential function of Fibonacci heap. [8]
  - (b) Explain the implementation of a binomial heap and its operation with suitable example. [8]

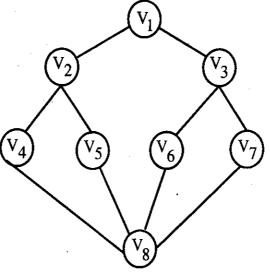
#### <u>OR</u>

- Q.2 (a) Show how to maintain, for every node of a 2-3-4 tree, the height of the subtree rooted at x as a field height [x]. Make sure that your implementation does not affect the asymptotic running times of searching, insertion, and deletion. [8]
  - (b) Show the Fibonacci heap that result from calling FIB-HEAP-EXTRACT-MIN, the maximum degree D (n) of any node in an n-node Fibonacci heap is O(log n).

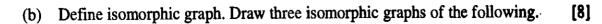
### <u>UNIT – III</u>

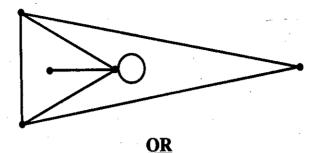
Q.3 (a) Define connected components of a Graph. For the given graph give the adjacency list.

[8]

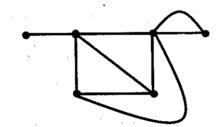


Write the BFS algorithm and traverse it starting from the vertex  $V_6$  showing various stages. How the connected components of a graph can be determined?





- Q.3 (a) Prove that for any vertex v other than the source or sink, the total positive flow entering v must equal the total positive flow leaving v. [8]
  - (b) Define cut-set vector and circuit vector of a graph. Find the set of all cut-set vectors and the set of all circuit vectors of the following graph: [8]



### UNIT - IV

- Q.4 (a) How many different zero-one input sequences must be applied to the input of a comparison network to verify that it is a merging network. [8]
  - (b) Consider two sequences of 0's and 1's. Prove that if every element in one sequence is at least as small as every element in the other sequence, then one of the two sequences is clean.

    [8]

#### <u>OR</u>

- Q.4 (a) Give a sequence of m MAKE-SET, UNION, and FIND-SET operations, n of which are MAKE-SET operation, that takes  $\Omega$  (mlog n) time when we use union by rank only. [8]
  - (b) Explain the following terms and their functioning:

[4+4=8]

- (i) 2-3 tree
- (ii) Concatenable Queue

[5700]

### <u>UNIT - V</u>

Q.5 (a) Prove that system (Z n, +n) and (Z\*n, .n) is a finite abelian group. [8]
(b) Prove that:

If n is an odd composite number, then the number of witnesses to the compositeness of n is at least (n-1)/2.

#### <u>OR</u>

Q.5 (a) Discuss Miller Rabin randomized primality test? [8]
(b) Give a brief review of notation of elementary number theorem? State division theorem. [8]

**SES107** 

Roll No. \_

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### 5E5107

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 Computer Science & Engineering 5CS6.2A Digital Signal Processing Common With CS, IT

Time: 3 Hours

Maximum Marks: 80

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

#### Instructions to Candidates:

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

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1. <u>NIL</u>

2. NIL

### <u>UNIT – I</u>

Q.1 (a) Check whether the following systems are linear -

[8]

- (i) F[x(n)] = an x(n) + b
- (ii)  $F[x(n)] = e^{x(n)}$
- (b) Check whether the following systems are linear & time invariant -

[8]

- (i)  $F[x(n)] = n[x(n)]^2$
- (ii)  $F[x(n)] = a[x(n)]^2 + 3(x(n))$

#### <u>OR</u>

Q.1 (a) List out the properties of LTI system. Explain each with the help of an example.

[5E5107]

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[2480]

(b) A second order discrete time system is characterized by the difference equation. [8] •

$$y(n) - 0.1y(n-1) - 0.02y(n-2) = 2x(n) - x(n-1)$$

Determine y(n) for  $n \ge 0$  when x(n) = 4(n) &

The initial conditions are y(-1) = -10 &

$$y(-2) = 5$$

### UNIT - II

Q.2 Figure 2 Q.2 The arconvolution of an FIR filter with impulse response  $h(n) = \{1, 2, 4\}$ 

.... .... ...... with padding of Zeros.)

[16]

#### <u>OR</u>

- Q.2 (a) Define ROCLE. Som. Write down its properties for Z transform. [6]
  - (b) Determine the inverse  $\angle$  cansform of the following x(z) by the partial fraction expansion method. [10]

$$\left[ x(z) = \frac{z+2}{2z^2 - 7z + 3} \right]$$

If the ROCs are

- (a) |z| > 3
- (b)  $|z| < \frac{1}{2}$
- (c)  $\frac{1}{2} < |z| < 3$

### <u>UNIT – III</u>

Q.3 Define sampling theorem. Explain Interpolation technique for ... signal from its samples. [16]

### <u>OR</u>

Q.3 (a) What do you mean by aliasing.

[6]

(b) A Continuous signal is given as  $x_e(t) = \sin(2\pi (100)t)$ 

This signal was sampled with sampling period T = 1/400 second to obtain discrete time signal x(n). Determine the resulting signal x(n). [10]

[5E5107] Page 2 of 3 [2480]

## UNIT - IV

Find the DFT of the sequence:

[10]

 $x(n) = \begin{cases} 1; 2 \le n \le 6 \\ 0; n = 0, 1, 7, 8, 9 \end{cases}$ 

Given N = 10

Explain Parseval's theorem & circular shift property for DFT.

[6]

#### <u>OR</u>

Explain Decimation in frequency FFT (DIF-FFT) algorithm; with diagram. Q.4 (a)

Determine the four point DFT for  $x(n) = \{0, 1, 2, 3\}$  using DIT - FFT [8] algorithm.

UNIT - V

Q.5 Write shot note on -

 $[4 \times 4 = 16]$ 

Structures of FIR filter

- Cascade & parallel structure
- Hamming window (c)
- Chebyshev filter

### <u>OR</u>

[16] Q.5 The following specifications are given to design a band pass filter -Stop band frequencies =  $0.1\pi$  rad/sec,

 $0.7\pi$  rad/sec.

Pass band lower cutoff frequency =  $0.25\pi$  rad/sec

Pass band upper cutoff frequency =  $0.35\pi$  rad/sec

Pass band attenuation = - 3dB.

Stop band attenuation = - 15dB

Sampling rate = 1 sample/sec.

Design a Band pass filter using bilinear transformation.

SE5101

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### -5E5101

B. Tech. V Sem. (Main/Back) Exam., Nov.-Dec.-2016 Computer Science & Engineering 5CS1A Computer Architecture Common with CS, IT

Time: 3 Hours

**Maximum Marks: 80** 

Min. Passing Marks Main: 26

Min. Passing Marks Back: 24

#### Instructions to Candidates:

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1. <u>NIL</u>

2. <u>NIL</u>

### UNIT - I

Q.1 (a) Write down the Flynn's classification of computer?

[8]

(b) What does pipeline, vector and array processor mean in parallel processing? [8]

m paramer processing?

### <u>OR</u>

Q.1 (a) Describe the Von - Neumann model and explain the functioning of its components. [8]

(b) Explain and draw a diagram of a bus system that use multiplex k, register of n bits each to produce an n - line common bus.

[5E5101]

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[7340]

## <u>UNIT – II</u>

[5E5101	1] Page 2 of 3	[7340]
<b>(b</b> )	Explain associative memory with its hardware organization. Disprocedure for reading and writing data in associative memory.	[8]
Q.4 (a)	cache coherency.	[8]
	What is cache coherency why is it necessary? Explain different appro	oaches for
	The normalized fraction Mantissa has 16 bits and be exponent has 8 bits	,. <sub>[</sub> o]
(b)	Represent the number (+46.5) 10 as a floating point binary number with the send he exponent has 8 bits	iii 24 viis. S. [8]
	number.	[8] th 24 hits
Q.3 (a)	Draw and explain flowchart for additional and subtraction of floati	ng points
( )	OR	_
(b)	Explain Booth multiplication algorithm and its hardware.	[8]
Q.3 (a)	Explain by use of Flowchart?	[8]
0.2 (a)	Describe the procedure for addition and subtraction for fixed point	number.
	be achieved?	[8]
•	speedup ratio of the pipeline for 200 tasks. What is maximum speedup	that can
(5)	processed in a six- segment pipeline with a clack cycle of 20ns. Determined the processed in a six- segment pipeline with a clack cycle of 20ns.	mine the
(b)	A non-pipeline system takes 100 ns to process a task. The same task	c can be
	systems.	[8]
Q.2 (a)	Discuss all factor which affect the performance of pipelining processor	
	<u>OR</u>	
` ,	the Register to a common bus.	[8]
<b>(b)</b>	Draw and explain the organization of a CPU showing the connections l	petween
(	(ii) Hardwired control unit	
(	(i) Address Sequencing	
Q.2 (a) H	Explain the following in detail:	[o]
		[8]

#### **OR**

Q.4 (a)	Explain the role of virtual Memory.	
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(b) Draw and explain the memory hierarchy in a digital computer. What are the advantages of cache memory over main memory? [8]

### <u>UNIT – V</u>

- Q.5 (a) List various commands that an interface may receive from control line of the Bus. Explain the process of handling an interrupt that occurs during the execution of a program, with the help of an example. [8]
  - (b) A DMA controller transfer 16- bits words to memory using cycle stealing. The words are assembled from a device that transmits character at a rate of 2400 characters per second. The CPU be is fetching and executing instruction at an average rate of 1 million instructions per second. By how much the CPU be slowed down because of the DMA transfer?

#### OR

- Q.5 (a) What is an interrupt service subroutine? How can the interrupt priority be resolved?
  - (b) Explain in short programmed I/O and interrupt initiated I/O.
  - (c) What do you mean by synchronous and asynchronous data transfer? Explain hand shaking method asynchronous data transfer? [16]

[7340]

[8]

Roll No. Total No of Pages: 3 5E5109 B. Tech. V Sem (Main/Back) Exam., Nov.-Dec.-2016 Imformation Technology 5IT6.2A E - Commerce Time: 3 Hours **Maximum Marks: 80** Min. Passing Marks Main: 26 Min. Passing Marks Back: 24 Instructions to Candidates: Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly. Use of following supporting material is permitted during examination. (Mentioned in form No. 205) 1. <u>NIL</u> 2. NIL UNIT -1 Q.1 (a) What is E - commerce? Explain the Generic trade cycle of e - commerce. [8] (b) Explain the Industry framework of e - commerce and various types of electronic commerce. [8] OR Distinguish between interorganization and intraorganization e - commerce. Q.1 (a) [8] (b) What do you mean by customer premises equipment (CPE)? Describe it with respect to set - top - boxes. [8] <u>UNIT - II</u> Q.2 (a) Explain the various driving forces and challenges of m - commerce. [8]

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[740]

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<ul><li>(b) Write short notes an:</li><li>(i) DMZ network</li><li>(ii) IP datagram.</li></ul>	<del>-</del>
(ii) IP datagram.	
(11) THE AMERICAN STREET	
<u>OR</u>	
Q.2 (a) What is WAP? Explain the WAP architecture in detail.	[8]
(b) Write short notes on:	$[2 \times 4 = 8]$
(i) Client server network security	·
(ii) Trust based security	•
(iii) Biometric system	
(iv) Worm	
<u>UNIT – III</u>	
Q.3 (a) Explain the various security principles in detail.	[8]
(b) Explain the terms data encryption and firewall with respect to securi	ity. [8]
<u>OR</u>	
Q.3 (a) How digital signature is different from digital certificates explain?	[8]
(b) Why we need VPN? Explain VPN architecture in detail.	[8]
<u>UNIT – IV</u>	
Q.4 Explain the following:	[16]
(a) Electronic payment and electronic money.	•
(b) Blinded money and binding factory.	
(c) Digital cash	
(d) ACID Test and ICES Test.	
<u>OR</u>	
Q.4 (a) What is use of SET? Explain SET process in detail.	[8]
(b) What are the key issues and challenges of online banking? Explain	. [8]
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## <u>UNIT - V</u>

Q.5	(a)	Explain the role of EDI trade exchange in the EDI transaction.	[ <b>7</b> ]
	(b)	Explain the following:	נין
		(i) Taxation issues.	[3]
		(ii) Cyber jurisdiction	[3]
		(iii) Encryption and Decryption laws.	
			[3]
		<u>OR</u>	
Q.5	(a)	Explain the difference between pull versus push supply chain management?	[8]
	(b)	Explain the architecture of CRM and architecture elements of a G	CRM
		solutions?	
•			[8]