2 (a) What is difference of Generate and concurrent statement ? Explain with suitable example.

8

(b) What is simulation and synthesis process in VHDL ?

8

UNIT - III

3 (a) Describe the steps of synchronous sequential circuit with suitable example.

8

(b) Explain Moore and Melay machine and describe the clock skew.

8

OR

3 Discuss the concept and working principle of following : (any four)

(i) ROM

(ii) FPGA

(iii) PLA

(iv) PLD

(v) Setup time and Hold time.

16

UNIT - IV

4 (a) What do you mean by event driven circuit ?

8

(b) Explain design procedure of asynchronous circuits.

8

OR