1 (a) Draw the block diagram for the hardware that implements $t + pq : A \leftarrow A+B$
where A and B are two n-bit resisters and t, p and q are control variables show the logic gate for the control function.

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(b) Design a N-bit combinational circuit decrementer using four full-adder circuits.

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UNIT - II

2 Write a program to evaluate the arithmetic statement :

$$X = \frac{A-B+C*(D*E-F)}{G+H*K}$$

(i) Using a general register computer with three address instruction.

(ii) Using a general register computer with two address instruction.

(iii) Using an accumulator type computer with one address instructions

(iv) Using a stack organized computer with zero-address operation instructions.

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OR

2 (a) The memory unit of a computer has 256 K words of 32 bit each. The computer has an instruction format with four field : an operation code field, a mode field to specity one of seven addressing modes, a register address field to specify one of 60 processor registers and a memory address. Specify the instruction format and the number of bit in each field if the instruction is in one memory word.

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(b) A computer has 32-bit instruction and 12-bit addresses. If there are 250 two address instruction, how many one address instruction can be formulated ?

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