

3E2075

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B. Tech. (Sem. III) (Main & Back) Examination, January - 2013
 Computer Engg. & Information Tech.
 3IT5 & 3CS5 Digital Electronics

Time : 3 Hours]

[Total Marks : 80
 [Min. Passing Marks : 24

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. (Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly. Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination.
 (Mentioned in form No. 205)

1. Nil

2. Nil

UNIT - I

1 (a) Prove the following :

(i) $A \oplus B = \bar{A} \oplus \bar{B}$

(ii) $\overline{A \oplus B} = A \oplus \bar{B} = \bar{A} \oplus B$

(iii) $B \oplus (B \oplus A \cdot C) = A \cdot C$

2×3=6

(b) Convert the following numbers from given base to the other base indicated :

(i) $(102.25)_{10} = (?)_2$

(ii) $(101.001)_2 = (?)_{10}$

(iii) $(736)_8 = (?)_2$

(iv) $(2F9A)_{16} = (?)_8$

(v) $(247.36)_8 = (?)_{16}$

5×2=10

OR

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[Contd...

- 1 (a) Convert the given code to other code :
- (i) $(327.89)_{10} = (\text{BCD})$ code
 - (ii) $(4096)_{10} = (\text{Excess} - 5)$ code
 - (iii) $(0100\ 0111)_{\text{BCD}} = (\quad ? \quad)$ gray code

3×2=6

- (b) Explain the following with one example :

- (i) Hamming distance
- (ii) Alpha numeric code.

2×2=4

- (c) Perform the following Addition/Subtraction :

- (i) $(54)_{16} - (2A)_{16}$
- (ii) $(123)_8 + (001)_8 + (203)_8$

2×3=6

UNIT - II

- 2 (a) Draw the circuit diagram of 3-input NAND gate using TTL logic and find the expression for fan out.

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- (b) Draw circuit for 2-input NOR using CMOS and explain its working. Also compare the advantage and disadvantages of CMOS logic with other.

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OR

- 2 (a) Define the following and give one example for each :

- (i) Propagation delay
- (ii) Wired logic
- (iii) Schottky diode clamping
- (iv) RTL logic.

4×2=8



- (b) What is difference between Saturation logic and Active logic. Explain these with one example and show their speed capability.

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UNIT - III

- 3 (a) Minimise the four variable logic function using K-map :

(i) $f(A, B, C, D) = \sum m(1, 2, 3, 5, 7, 8, 9, 11, 14)$

(ii) $f(A, B, C, D) = \prod m(4, 6, 10, 12, 13, 15)$

4×2=8

- (b) Simplify the following logic expression using K-map and implement them using NAND gate :

(i) $Y = (A + \bar{B} + C)(\bar{A} + \bar{B} + \bar{C})(\bar{B} + \bar{C} + D)$

(ii) $Y = ABC\bar{D} + \bar{A}BCD + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{D} + \bar{B}$.

4×2=8

OR

- 3 (a) Minimise the following expression with don't care conditions using K-map :

(i) $Y = \sum m(1, 3, 7, 15) + d(0, 2, 5)$

(ii) $Y = \prod m(4, 5, 6, 7, 8, 12) + d(0, 1, 2, 9, 11, 14)$.

6×2=12

- (b) Explain the Quinn-Mcklusky minimization technique with one example.

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UNIT - IV

- 4 (a) Design a Gray-to binary code converter logic circuit.

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(b) Implement the following logic expression using multiplexer :

(i) $Y = \sum m(1, 2, 3, 5, 6)$

(ii) $Y = \prod m(0, 1, 2, 5, 7)$.

4×2=8

OR

4 (a) Design a BCD to Excess-3 encoder.

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(b) Realise the following :

(i) $Y = \sum m(0, 1, 2, 3, 11, 12, 14, 15)$ using 16 : 1 multiplexer.

(ii) $Y = \prod m(0, 1, 3, 7, 9, 10, 11, 13, 14, 15)$ using 4 to 16 line decoder.

4×2=8

UNIT - V

5 (a) Convert the following :

(i) J-K FF to S - R FF

(ii) D FF to J-K FF.

4×2=8

(b) Draw the logic circuit for Asynchronous modulo-10 counter and draw its waveform :

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OR

5 (a) Draw the state diagram of :

(i) JK FF

(ii) 4 bit binary counter.

4×2=8

(b) Design a sequence detector to detect a serial input sequence 1010. Draw its state diagram, state table, state assignment table and final implemented circuit.

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