305

3E1461

Roll No. : _____ Total Printed Pages : 3

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B. Tech. (Sem. III) (Reback) Examination, February - 2013
Computer Engg.
3CP/CS1(O) Digital Electronics (Common for CP & IT)

Time : 3 Hours] [Total Marks : 80

[Min. Passing Marks : 24

Attempt any five questions, selecting one question from each unit. All questions carry equal marks. Schematic diagrams must be shown wherever necessary. Any data you feel missing suitably be assumed and stated clearly.

Units of quantities used/calculated must be stated clearly.

Use of following supporting material is permitted during examination. *(Mentioned in form No. 205)*

1. NIL 2. NIL

UNIT - I

1 (a) Convert hexadecimal 2AC5 to binary, octal and decimal.

(b) Determine value of base x if $(193)_x = (623)_8$.

(c) Represent $(8)_{10}$ with 7421, 8421 and 84(-2)(-1).

(d) What do you mean by self-complementing code. Explain with example.

16

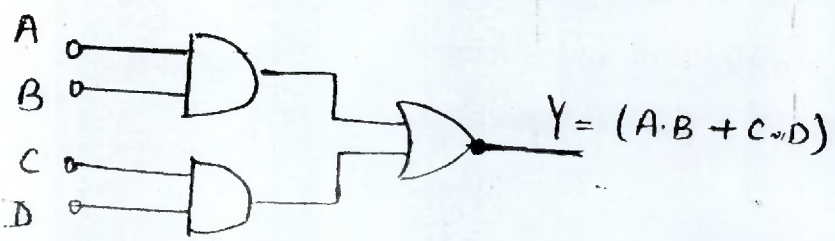
OR

1 (a) Implement EX-OR logic operation with only NAND gates.

(b) Using Boolean Algebra show that

$AB+AC+\bar{B}C = AB+\bar{B}C$

(c) Implement using NAND gates only.



(d) Simply and draw circuit

$$\left(\overline{\overline{A+B}+\overline{A+\overline{B}}}\right)+\overline{\left(\overline{\overline{A}B}\right)\left(\overline{A\overline{B}}\right)}$$

16

UNIT - II

2 (a) Minimize the following using Quise-Meclusky method and realise using NAND/NOR gates

$$f(A,B,C,D)=\sum m(2,3,6,7,8,9,13,15)+d(4,10,12)$$

8

(b) (i) Express the boolean function in the product of maxterm form

$$F = AB+\overline{A}D$$

(ii) Obtain the minimal POS form using K-map

$$F(A,B,C,D)=\sum m(0,1,2,5,8,9,10)$$

8

OR

2 (a) Minimize the following 4 variable function using K-map and implement it in universal logic.

(i) $f_1=\pi_m(0,2,6,10,11,12,13)+d(3,4,5,14,15)$

(ii) $f_2=\sum m(0,2,3,4,6,8,10,11,12,13,14)+d(1,15)$

8

(b) Define the following :

(i) Minterm and Maxterm

(ii) Incompletely specified functions.

8

UNIT - III

3 (a) Design a BCD to decimal decoder by solving K-map and make a suitable ckt diagram.

(b) Draw the full adder using two half address and obtain the expression for sum and carry.

8+8

OR

3 (a) Implement the following function using 4:1 mux

$$f(A,B,C,D) = \sum m(2,4,6,7,9,10,11,12,15)$$

(b) Design a gray code to binary code converter and realize it using AND/OR/NOT gates.

8+8

UNIT - IV

4 (a) Realize a mod-5 counter using JK Flip Flop by showing the truth table and a suitable diagram.

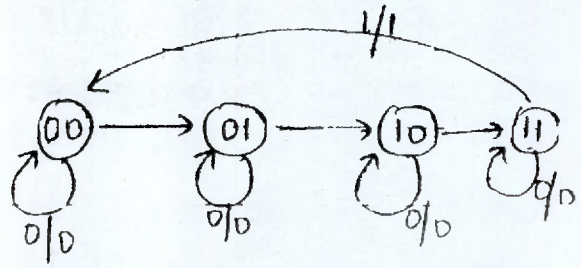
(b) Realize T Flip Flop from JK Flip Flop.

8+8

OR

4 (a) Differentiate between asynchronous and synchronous sequential circuits.

(b) Derive the flipflop ckt to represent state diagram given below.



8+8

UNIT - V

5 (a) Explain Totem pole arrangement in TTL. What is the advantage and disadvantage of this arrangement ?

(b) Explain and realize 2-input NAND and NOR gate in CMOS logic.

8+8

OR

5 (a) Explain the following characteristics of logic family

(i) Propagation delay

(ii) Power dissipation

(iii) Noise Immunity

(iv) Fan-in and Fan-out

(b) Explain the interfacing of logic families.

8+8
