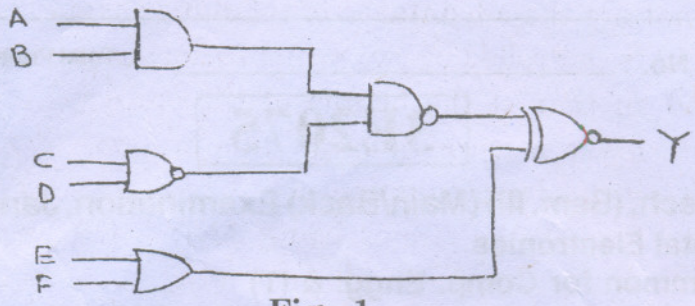

Fig. 1

8

UNIT-II

2 (a) Define the (i) noise immunity and (ii) Fanout. Draw the internal structure of TTL tristate gate and explain its operation.

8

(b) Explain the parameters used to characterize logic families. Calculate the noise margin of ECL gate.

8

OR

2 (a) Draw the circuit for CMOS inventer. What are the different schemes for CMOS to TTL interface. Explain one of them.

8

(b) Explain how a MOS can be used as a switch in a digital circuit ? How does a TTL gate differ from MOS gate ?

8

UNIT-III

3 (a) Obtain minimum SOP expression for following Boolean expression using Karnaugh Map.

$F = \sum m(0,1,2,5,7,9,13,15) + d(8,11)$

Realise the minimised function using logic gates.

8

(b) Implement the following boolean function with NOR-NOR gate logic.

$Y = AC + BC + D$

8

OR

3 (a) Explain briefly the systematic procedure for using don't care condition. Define multilevel logic circuit with diagram.

8